Improved CD control for 45/40nm CMOS logic patterning. Anticipation for 32/28nm.

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ABSTRACT

Since 2008, we have been presenting some papers regarding CMOS 45nm logic gate patterning activity to reduce CD dispersion. After a global CD budget evaluation at SPIE08 [1], we have been focusing on Intrafield CD corrections using Dose Mapper™[2]. The story continues and since then we have pursued our intrafield characterisation and focus on ways to get Dose Mapper™ dose recipe created before the first silicon is coming. In fact 40nm technology is already more demanding and we must be ready with integrated solutions for 32/28nm node.

Global CD budget can be divided in Lot to Lot, Wafer to Wafer, Intra wafer and Intra field component. We won't talk here about run to run solutions which are put in place for Lot to Lot and Wafer to Wafer. We will emphasize on the intrafield / intrawafer process corrections and outline process compensation control and strategy. A lot of papers regarding intrafield CD compensation are available in the litterature but they do not necesserally fit logic manufacturing needs or possibilities. We need to put similar solutions in place which are comprehensive and flexible. How can we correct upfront an Etch chamber CD profile combined with a mask and scanner CD signature? How can we get intrafield map from random logic devices? This is what we will develop in this paper.

Keywords: Photolithography, Immersion, Optical CD, Mask, Intrafield, Dose Mapper^{TM}, Aerial Image, Etch compensation, WLCD32, CDC^{TM}200.

1. INTRAFIELD CD CHARACTERISATION & COMPENSATION FOR LOGIC

1.1. Mask metrology

For logic circuit is highly random, once tape out is assembled, the reticle assembly team extracts a metrology file location to be measured by mask shop. These sites are identified as Circuit / Intrafield Blocs / Frame structures. This extraction is based on given design rule description or markers.

Depending on Mask Grade and layer, the number of measured point can vary as well as dispersion specs such as mean / min / max / 3sigma deviation to target.

All these datas are gathered in a certificat of acceptance, compiled in a database.

The charts below show examples of such data collection made on masks (one product several layer in this case).

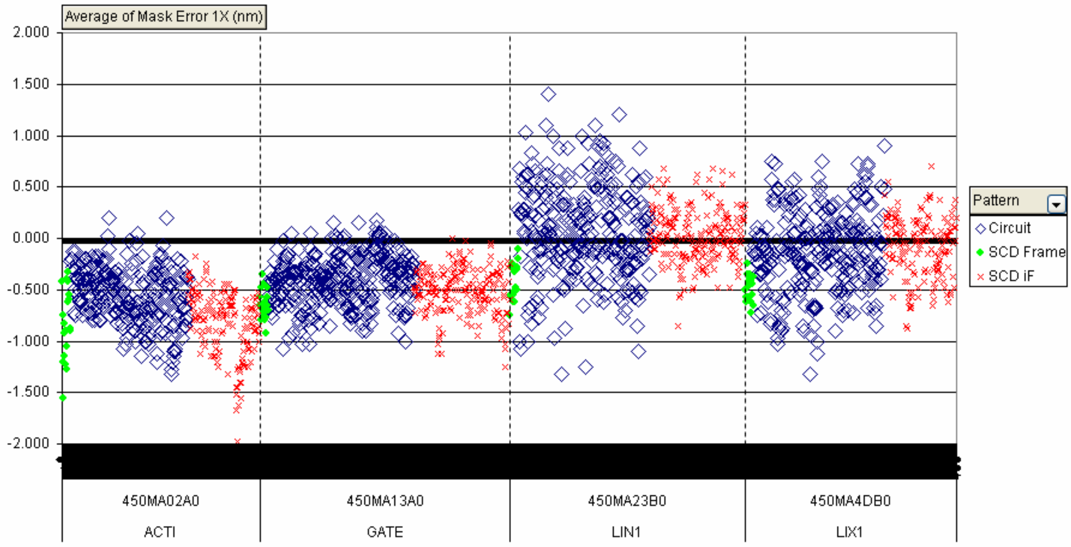


Figure1: Representation of mask CD delta to target datacollection of 4 different masks

1.2. Intrafield target placement

We have started to put inside the field some intrafield targets that can be measured in-line to ensure good process control. One of the question was : Are they representative enough of the circuit behavior?
Here are two examples of in field CD extraction location:

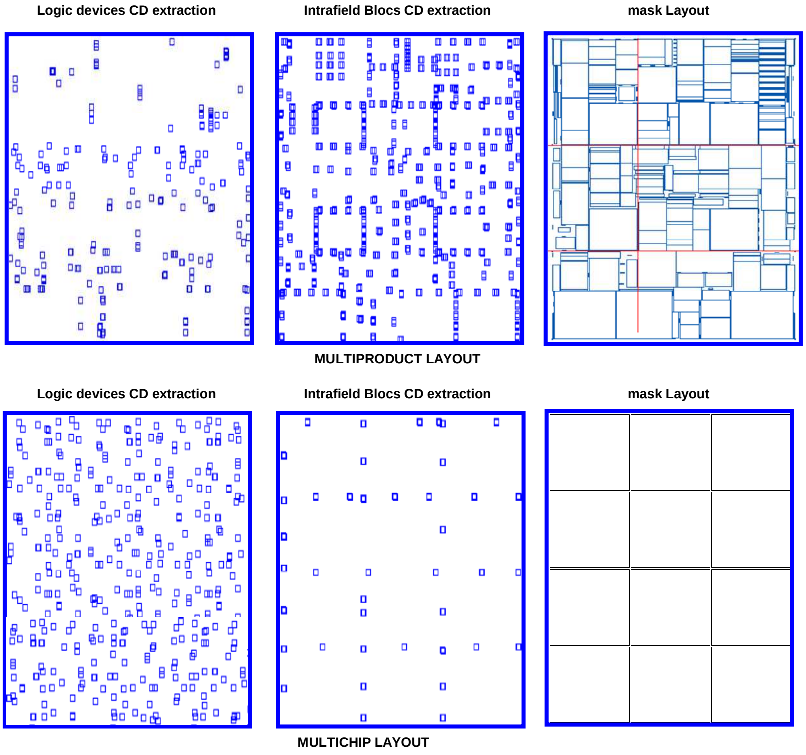


Figure2: Illustration of 2 cases of Intrafield target positioning (top) Multiproduct mask (bottom) Multichip Mask

It is easy to highlight from these 2 observations the difficulty to put Intrafield control blocs in the field of the mask. Since we cannot easily find repetitive structures in a logic circuit, we need to find a way out to place process control blocs in the chip. Most of the time the designers will tend to fill the chip as much as possible. However there are always spaces left between IP blocs where dummy structures are usually placed. Can we use this space to place some metrology targets? What is the correlation between the size of a bloc and the probability to place one or more inside the chip?
This exercize was done on a production chip. We see from the trend that, as expected, the smaller the feature the higher the placement opportunities are. In practice we saw that there is quite some room available for what we need on a logic chip.

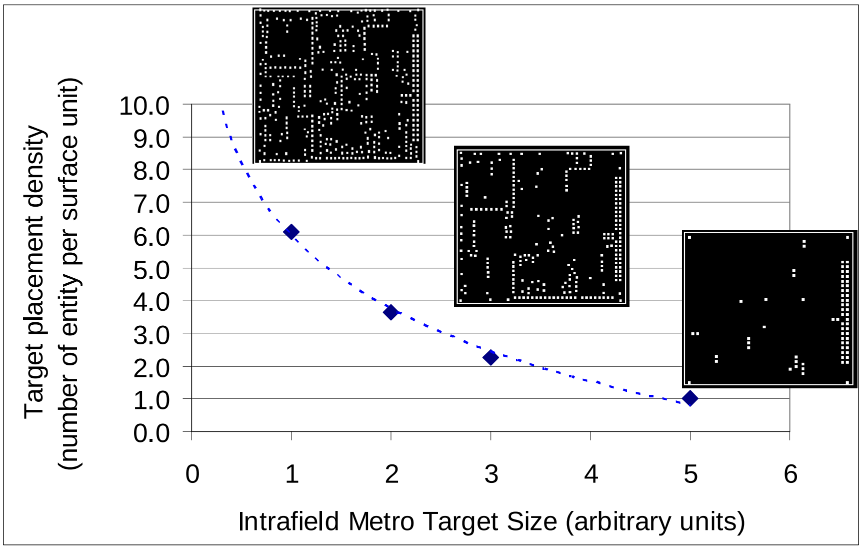


Figure3: Intrafield target placement in a chip as a function of their size.

1.3. Intrafield blocs representativity

The important thing is to also check whether the intrafield blocs are representative of the circuit CD behavior or not. If we look at the mask data from an intrafield site position perspective, we see that basically the intrafield blocs (when designed correctly) do follow the CD trend observed in the circuit. We can see a slight shift in the average but nevertheless the trend response is there, and we can consider that the intrafield blocs information is relevant enough for intrafield CD control.

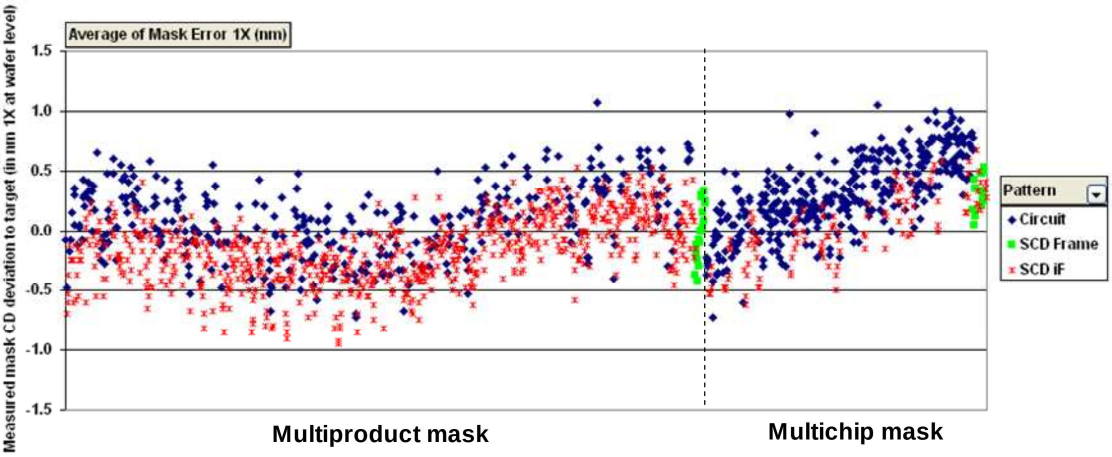


Figure 4: Mask CD delta to target datacollection of a GATE mask corresponding to sampling plan shown figure2.

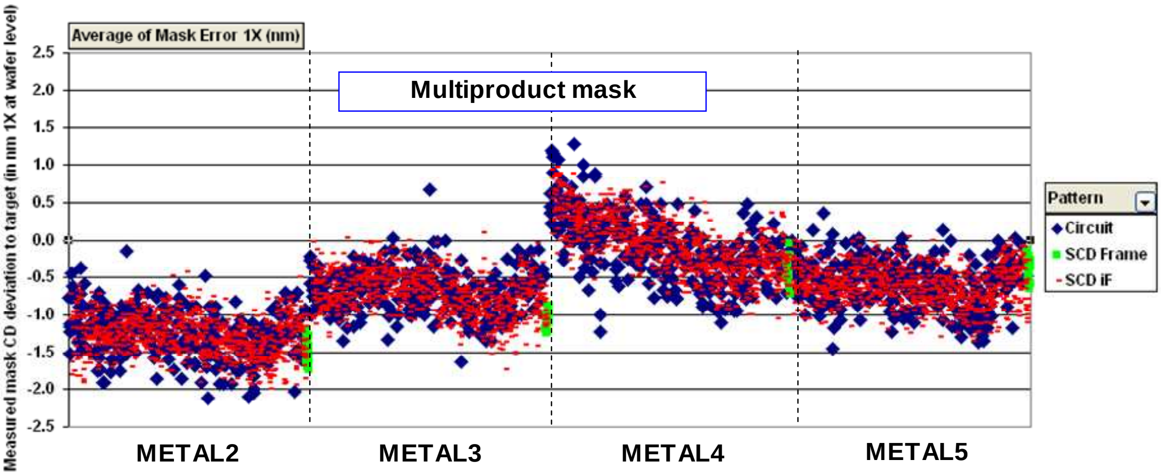


Figure 5: Mask CD delta to target datacollection of METAL masks corresponding to the same multiproduct mask shown at GATE previously.

We have possibilities to connect data from one intrafield bloc to the closest circuit measurement point. This allows us to display correlation. On the graph below we correlates the CD of intrafield blocs versus the closest circuit measurement within 250µ at mask level.

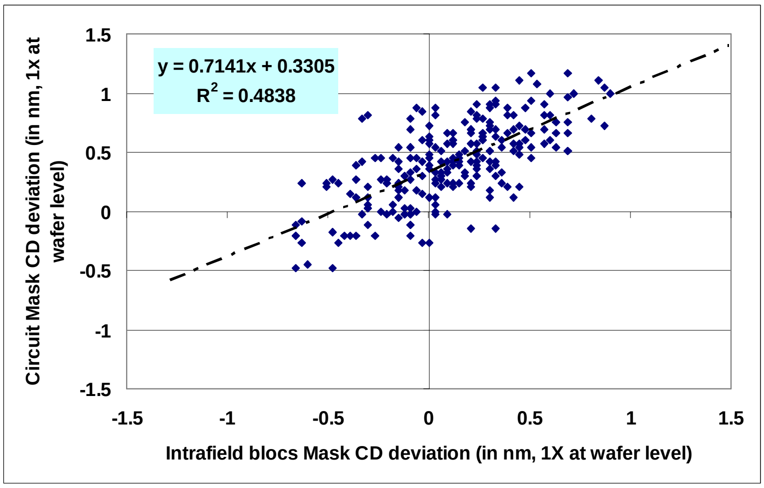
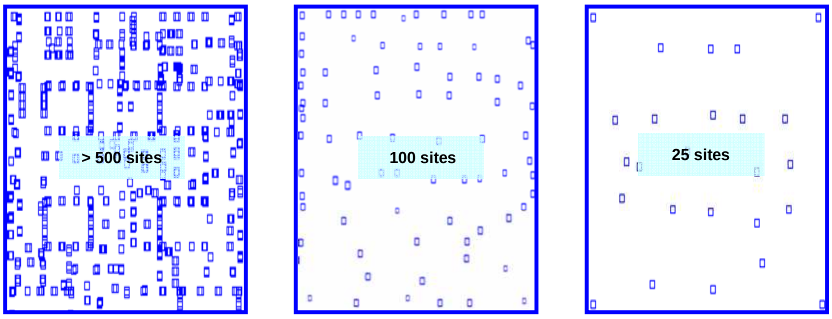


Figure 6: Correlation "site to site" between Intrafield blocs and circuit for a GATE mask

With these kind of data, the measurement noise level is not optimum since it is all measured using CDSEM (no choice yet for random circuit features). We'll see further in this paper that Aerial Imaging CD metrology is more relevant to perform mask to silicon CD correlation. Anyway we wanted to show that somehow the intrafield blocs placed in the field for process control give at first order a relevant information.

1.4. In-Line CD control

All these intrafield targets we place, are potential points to be used for in-line control. However for capacity and throughput reasons we will measure on lot only few of them (say a maximum of 25). As an example, for the process control strategy, we can have the sampling decomposition shown figure7.



All MASK Metrology **Intrafield CD blocs** **In-Line metrology Intrafield CD blocs**

Figure 7: Example of different subgroups of intrafield metrology blocs

From these 25 sites, we can then monitor the intrafield in-line with good confidence to overall field CD.

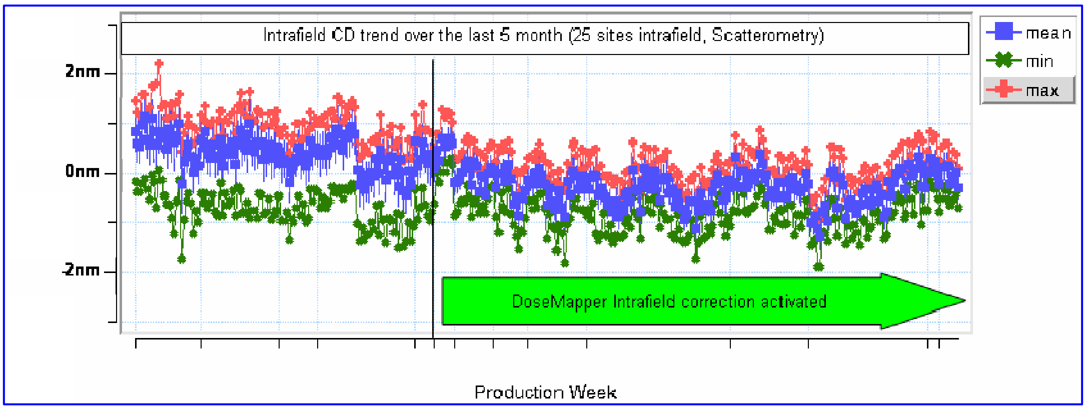


Figure 8: Intrafield CD data collection trend for 40nm node (Gate level)

It is more interesting to look at this trend from a CD dispersion point of view. On figure 9, we have plotted the CD range (per wafer/lot) in nanometer of these 25 intrafield blocs. We see that the intrafield trend is quite stable and when we have started to perform intrafield CD corrections with Dose Mapper™, a gain of 0.75nm equivalent to 45% of intrafield CD dispersion can be clearly demonstrated.

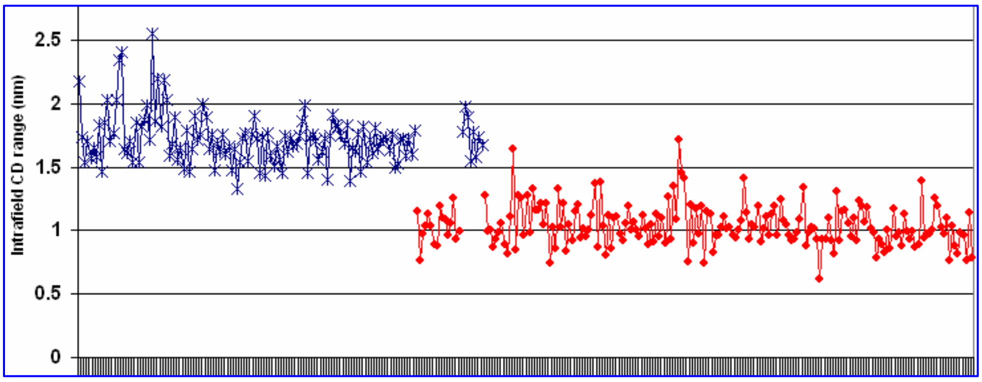


Figure 9: Intrafield CD dispersion (range in nm) of 40nm GATE (blue before Dose Mapper™ correction / Red after)

From these charts, we can show in-line patterning process improvement using Dose Mapper™. However the most important is to see whether it also worked on electrical structures. We mentioned earlier that intrafield blocs had enough correlation with circuit metrology to be significative enough. We need to confirm this with another sensor. In the mask set, we also have intrafield electrical CD structures which have another layout than the blocs. On the figure below we see the intrafield dispersion trend of such structure before and after Dose Mapper™ deployement. The dose recipe has been made from intrafield blocs set, but naturally applies to all features. Like in-line photo CD data, we see an improvement of 35% (note that here, we compare a population of 9 in-line electrical CD sites on figure 10 versus 25 in-line Scatterometry CD sites on figure 9).

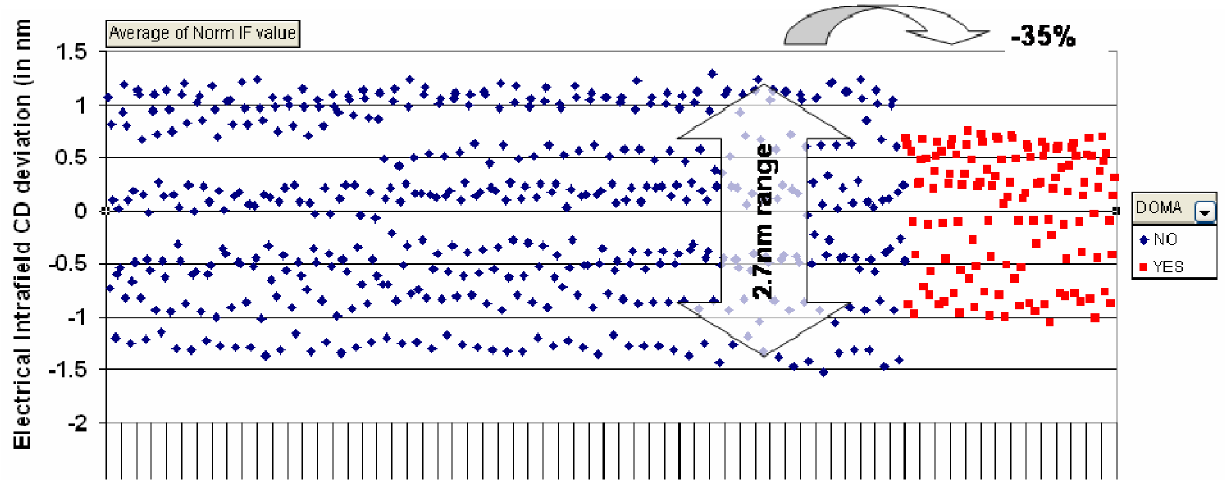


Figure 10: Intrafield ElectricalCD (in nm) of 40nm GATE (blue before Dose Mapper^{TM} correction / Red after). In-Line parametric trend (normalized per field)

1.5. New needs of Mask metrology

Up to now we were talking of CDSEM mask metrology. However from all the SEM data we had, we couldn't easily get accurate enough informations to generate a performant intrafield dose recipe. So far, dose recipes were generated by measurements on lot, so with needs of pilot wafers! The reason is that we couldn't get good correlation between mask CDSEM metrology and silicon scatterometry CD data (SCD) (R^2 is only 0.4 as seen on figure11). CDSEM information only gives back CD data from MoSi or Cr layer but doesn't take into account substrate or phase error. This why we have started evaluation of aerial imaging CD metrology of our masks starting with GATE layer.

For this we have used the newly developed WLCD32 tool from Zeiss and performed the following experiment:

- CDSEM metrology of intrafield blocs at MaskShop
- Mask exposure on lot on fab site
- Mask Aerial Imaging metrology at Zeiss place on WLCD32 ([3], [4])

We have then compared one to one CD datas.

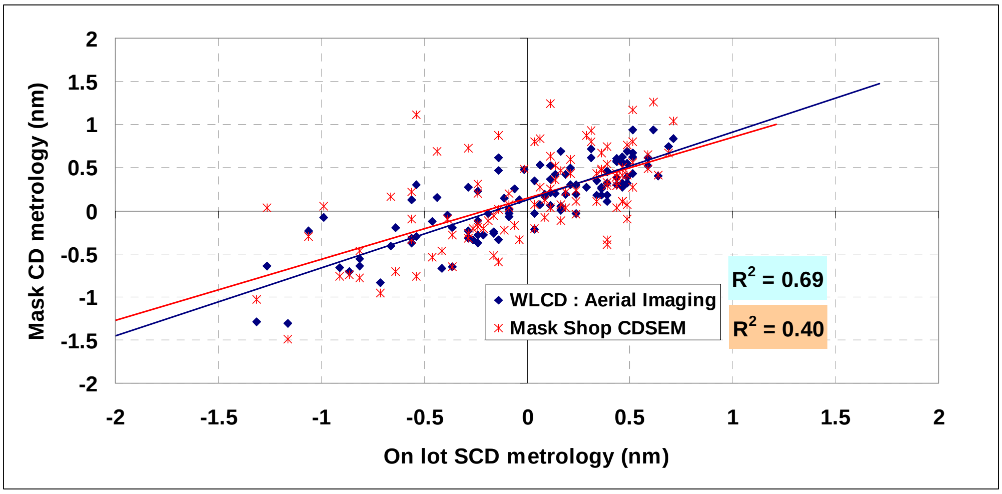


Figure 11: Intrafield CD correlation between Scatterometry on lot metrology and mask maskshop CDSEM metrology and WLCD32 Zeiss Aerial Image metrology.

We see, on this graph, that moving to aerial imaging CD metrology, silicon to mask correlation is significantly improved and R² reaches 0.69. This leads to a set of information which starts to be relevant enough for dose recipe creation.

1.6. Intrafield feedforward CD metrology

The idea for us is to be able to generate intrafield dose recipe before we process the first wafers. We just saw from figure 11 that aerial imaging CD metrology is giving good mask information. When we looked deaper in the data we also saw that there are some points in the field giving excellent correlation while others show CD discrepancy.
In fact, the intrafield CD is expected to be a composite of the mask and the scanner. We have then performed scanner intrafield CD characterisation and have added the result to the aerial image mask CD data collected with WLCD32 tool , as well as CDSEM data from maskshop (for comparison)
From the same data set, when including scanner dispersion we achieve then a correlation factor between “predicted” intrafield CD (say Mask CD data measured by WLCD32 Aerial Imaging + Scanner Intrafield CD deviation) of 0.91. This is a very good results saying that from now, we can derive a dose recipe for intrafield CD correction by using mask aerial image CD combined with scanner monitor data. Note that with mask CDSEM data the correlation is not bad either saying the scanner fingerprint is also quite significative.

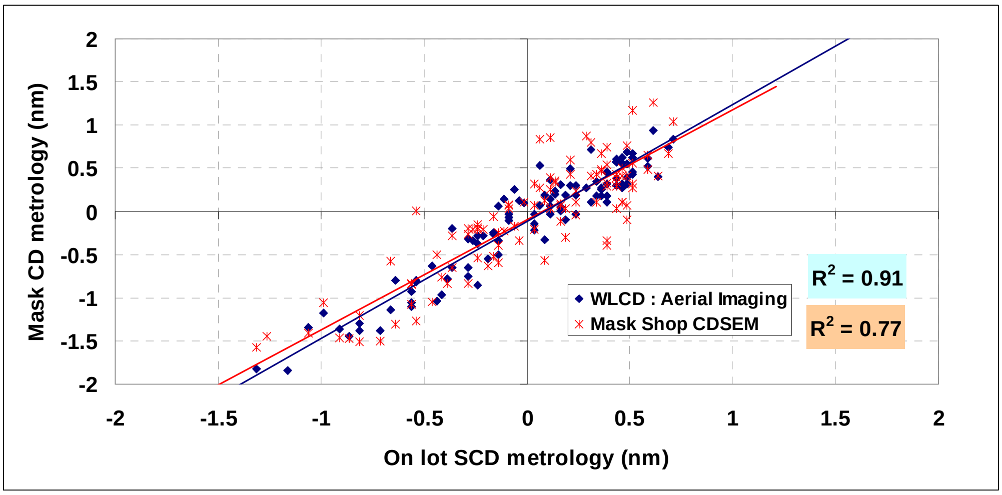


Figure 12: Intrafield CD correlation between Scatterometry on lot metrology and mask maskshop CDSEM metrology and WLCD32 Zeiss Aerial Image metrology.(WLCD32 & CDSEM masks data corrected from Scanner intrafield CD dispersion)

1.7. Pixer-CDC^{TM}200 mask correction and WLCD32 aerial imaging

We just mentioned that aerial imaging CD metrology combined with intrafield scanner footprint characterization, gives enough information to predict on lot intrafield behavior. This means for example, that when using Dose Mapper™ tool we need to combine two intrafield signatures (mask & scanner) for intrafield corrections. This makes the system a bit more complex but still manageable.

If we look ahead, mask shops are pushed to get perfect recticles. Even though we have some process correction options, any means which can help to reduce as much as possible the mask CD fingerprint is welcome. With a perfect mask we would only have to take care of the scanner part.

The Pixer company did develop a process to correct for mask CD deviation [5],[6]. Combined with WLCD32 aerial imaging CD, some evaluation was done to correct for a logic GATE mask with such process.

On figure 13, aerial image CD maps are reported before and after CDC^{TM}200 process correction. On these data, an intrafield CD dispersion reduction of 40% is observed on the mask.

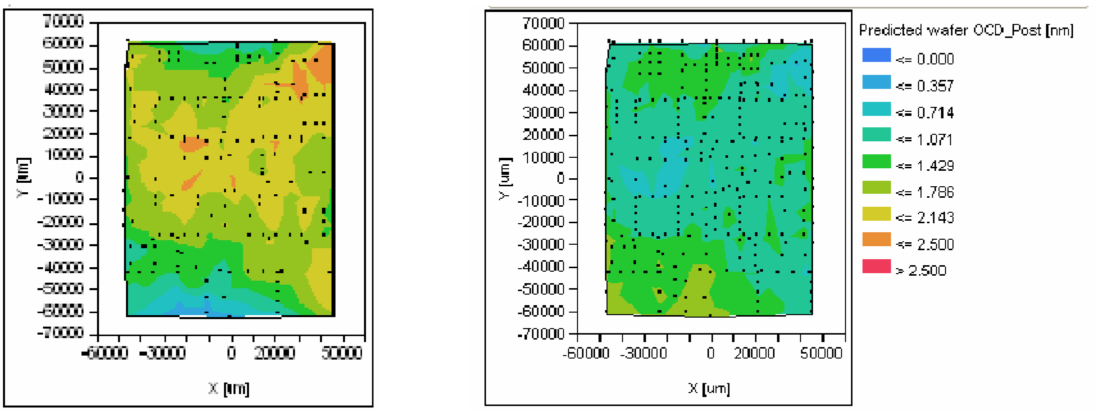


Figure 13: Intrafield CD WLCD32 Aerial Image map before (Left) and after (right) mask CDC^{TM}200 correction.

This mask has been exposed and measured in fab before and after CDC^{TM}200 correction, so that we can, in both cases, compare WLCD32 and silicon scatterometry data. Figure 14 reports WLCD32 versus SCD correlation before and after CDC^{TM}200 correction and figure 15 reports the compared intrafielf CD uniformity gain.

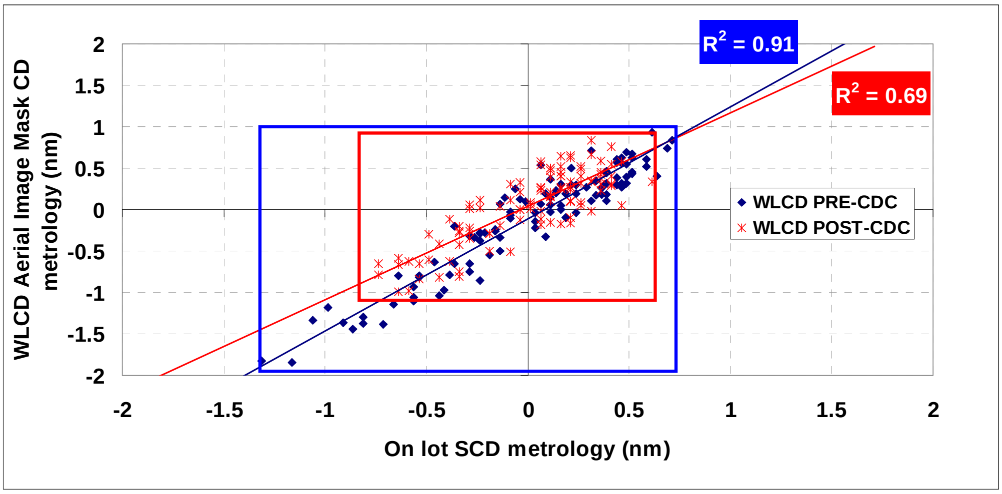


Figure 14: Mask WLCD32 vs on lot Scatterometry correlation, before and after mask CDC^{TM}200 correction.

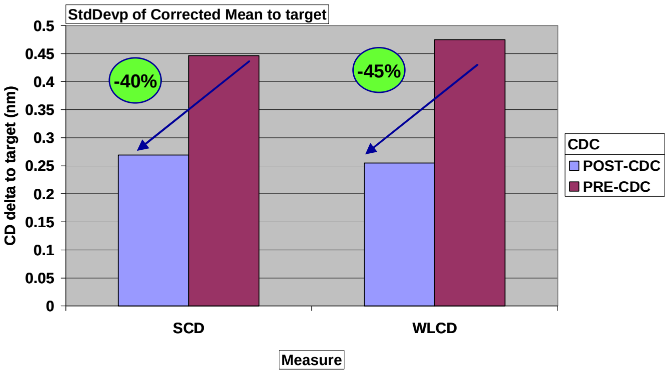


Figure 15: Observed Intrafield CDu improvement using CDC^{TM}200 process, measured by WLCD32 & Scatterometry.

In this data set, scanner intrafield effect has not been corrected. Still, the very interesting part of this experiment is that WLCD32 metrology is predictive even after CDC^{TM}200 correction. We have a residual scanner intrafield CD uniformity signature which could be corrected by a complementary Dose Mapper™ subrecipe!

The fact is that CDC^{TM}200 and Dose Mapper™ are complementary. There will be some scanner contribution correction to do anyway and, as we will show, intrawafer correction as well.

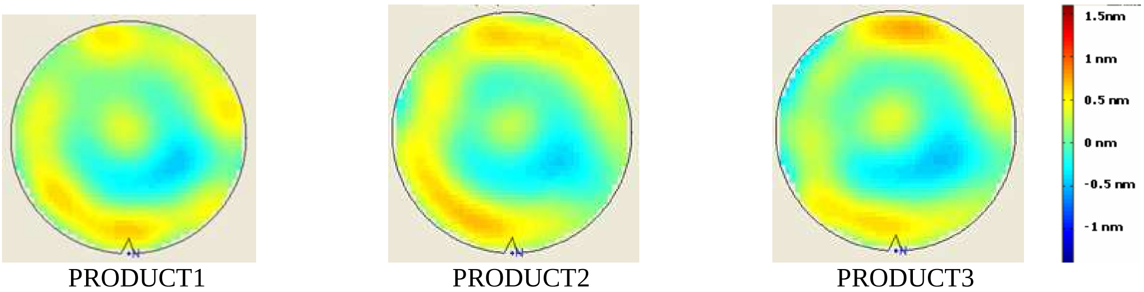
2. INTRAWAFER CD CORRECTION (ETCH COMPENSATION)

Like intrafield, it is also possible to evaluate the intrawafer process signature and correct for it using Dose Mapper^{TM}. We keep the same idea of processing a lot with an intrawafer dose recipe without doing any kind of pilot wafer. In other words, we don't want to have, if possible, intrawafer dose recipe product or tool dependant. For this we need to characterize the etch process and identify the process signature which is common to all tools and product.

So for a given etch recipe, corresponding to a given context : technology / layer, we have made a significant amount of fullmap etch bias characterization.

We have to say that, in parallel to this work, consequent process improvements were implemented to minimize the product effect and optimize intrinsic etch process CDu. Our perception is that Dose Mapper^{TM} is not to be deployed without a proper well characterized process. So, we could end up to an etch profile signature independent of the Etch chamber (from a same type) and the product.

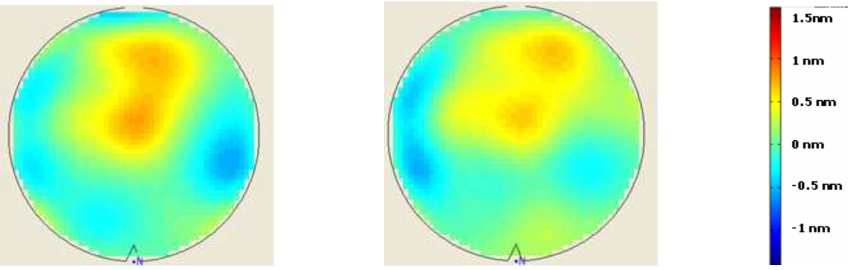
First on a given chamber we have looked at the product intrawafer CD uniformity effect (here on 45nm node)



PRODUCT1 PRODUCT2 PRODUCT3

Figure 16: Intrawafer CD map for Etch GATE in 45nm node for 3 different products.

It is quite clear from these maps that the process behaves the same way for these products. Then for a given process product, we have compared the etch chambers and looked for the common signature. For figure17, it concerns this time the 40nm Etch process.



ETCH CHAMBER 1 ETCH CHAMBER 2

Figure 17: Intrawafer CD map for Etch GATE in 40nm node for 2 differents Etch tool.

Again, we see almost no differences between these 2 chambers. Making a site to site correlation gives a R² > 0.7. From this data set (product and chamber effect: for the same etch recipe/technology) we derive an etch profile which is being used for any new product coming into process. For intrafield we could manage to get in-line control, we also need then to monitor in-line the behavior of the etch process so that dose recipe correction always fits process behavior. This can be done by regular fullmap sampling.

Today, after several month of running process with Dose Mapper^{TM} etch CD bias uniformity compensation (mixed or not with intrafield), we see that the final etch CD uniformity is stable and performs well like seen of figure 18.

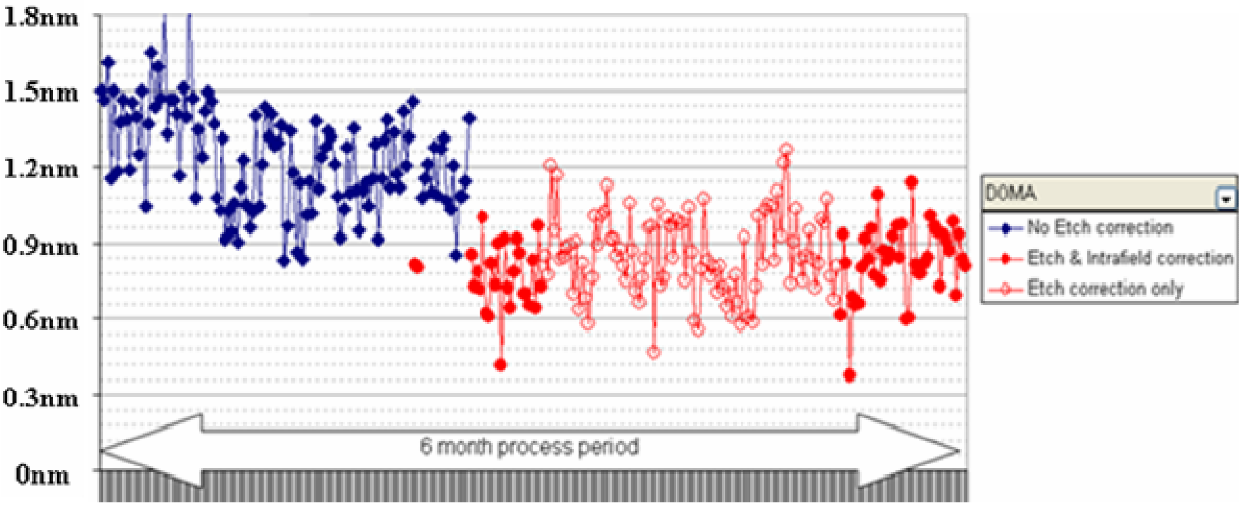


Figure 18: Intrawafer CD uniformity trend for Etch GATE in 40nm > 30% CD dispersion reduction with Dose Mapper^{TM} (3sigma < 1nm)

3. CONCLUSION

The process control requirements are getting more and more challenging. Process tools are improving but we are now in a situation where every nanometer and even tenth of nanometer counts. Along with process tools, process correction options are being developped. These plateforms like Dose Mapper™ (and mapper in general) or CDC^{TM}200 need the right input at the right time.

CDC^{TM}200 correction is a one shot correction needing quite some calibration work. Dose Mapper^{TM} is flexible but needs more automation. From end user side, we need to draw a comprehensive model of our CD variation and propose an adapted metrology and control plan.

Intrafield metrology is not that trivial. Spreading in-line control plan inside the field is not easy for logic device makers. We showed that there are some possibilities. By deploying the right control plan, we can safely setup intrafield process compensation tools.

For 40nm node we have shown a stable < 1nm 3sigma intrafield and intrawafer CD variation which is in fact on target for 32/28nm and on the good way for 22/20nm node.

When double patterning will come into the loop, we will need to have solutions in place. This means that these solutions must be tested and proven today on single patterning architecture.

In this paper we presented the following achievements:

1) Placing relevant intrafield control blocs into the field does give good feedback on random circuitry.
2) These control blocs allows us to evaluate WLCD32 Aerial Imaging and we have shown that it is the right metrology for mask CD to predict the silicon intrafield CD correctly.
3) Intrafield is not only mask, but combining mask aerial imaging CD with scanner intrafield CD profile is really predictive for silicon.
4) Dose Mapper^{TM} and CDC ^{TM}200 both brings about 40% intrafield CD uniformity improvement. We expect that a combination of both tools will provide the best CDu achievable.
5) On top of intrafield, Dose Mapper^{TM} brings > 30% intrawafer CDu improvement.
6) When properly characterized, we can generate subrecipes which can be used for month without updates.

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