

# Application of Pixel-based Mask Optimization Technique for High Transmission Attenuated PSM

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## ABSTRACT

Sub-resolution assist features (SRAF) insertion using a mask synthesis process based on pixel-based mask optimization schemes has been studied in recent years for various lithography schemes, including 6% attenuated PSM (AttPSM) with off-axis illumination such as Quasar. This paper will present results of the application of the pixel-based optimization technology for 6% and 30% AttPSM cases, using random contact hole patterns to compare and examine imaging properties of MEEF, CD uniformity, and side-lobe printing. We will also discuss practical techniques for manipulation of complex shapes generated by the pixel-based optimization to address mask manufacturability issues.

**Keywords:** inverse lithography, sub-resolution assist features, high transmission attenuated PSM, MRC

## 1. INTRODUCTION

Sub-resolution Assist Feature (SRAF) insertion using a mask synthesis process based on pixel-based mask optimization schemes known as inverse lithography (IL) has been studied [1] and experimented with in recent years for various lithography schemes, including 6% attenuated PSM (AttPSM) with off-axis illumination such as Quasar [2]. Detailed experimental investigation on the application of inverse lithography techniques for Quasar illumination with 6% as well as 30% AttPSM background was also conducted recently using AIMS<sup>TM</sup>-45 [3]. Potential benefits of high transmission schemes, such as lower mask error factor at dense pitches, have been well known for many years [4], but practical application of the high transmission schemes for random logic designs have been challenging, due to side-lobe printing issues. This paper will present further results of the application of pixel-based optimization technology to insert SRAF's to achieve intensity level uniformity, as well as to suppress side-lobe printing, for high transmission schemes.

We treated Contact Hole (CH) patterns drawn at pitches down to 116nm with pixel-based mask optimization for 6% and 30% AttPSM, and fabricated masks with these patterns. We show that pixel-based mask optimization is a way to avoid the critical chrome patterning normally used in tri-tone high-transmission masks, since the background printability can now be controlled by the placement of assist features. We assessed (both by simulation and exposure at NA 1.35) how the imaging can be controlled with the 30% AttPSM for regular and random CH geometries. Also, we examined whether or not the 30% AttPSM offers lower mask error factor and better CH uniformity on wafer than 6% AttPSM.

While the pixel-based optimization technique is well suited for SRAF insertion for such complex purposes, its use of contiguous short edges with arbitrary angles tends to break a variety of rules regarding mask manufacturability rules check (MRC). To construct mask shapes that pass the mask manufacturability constraints, a necessary first step is to simplify such complex mask shapes using only orthogonal and/or 45-

degree edges, while preserving the raw shapes as much as possible. However, the simplification process alone does not achieve full MRC-compliance. It takes additional steps to render the results MRC-clean with specific MRC rules such as minimum spacing, minimum area, and minimum fragment length. We will discuss practical techniques to iteratively transform the geometries for better compliance of each of these rules while utilizing the geometrical simplification as the central hub of the overall process to manage the complexity of the entire problem.

## 2. 30% ATTPSM AND INVERSE LITHOGRAPHY

A high transmission attenuated reticle offers the advantage of lower MEEF as well as better exposure latitude. Roughly 20-30% better MEEF is anticipated with 30% AttPSM (Figure-1). However, due to the high background transmission of 30%, the background will print under nominal conditions. Side-lobe printing is also a concern. Conventionally, chrome mask patterns have been used in such a way that a) chrome was placed close to 30% AttPSM edges to prevent background printing and b) chrome was placed around anywhere side-lobe printing could happen. This results in tri-tone masks, with two critical patterning steps in mask making. Our goal is to apply inverse lithography to suppress background printing and come to one patterning step on mask for 30% AttPSM, while keeping the benefit of lower MEEF.

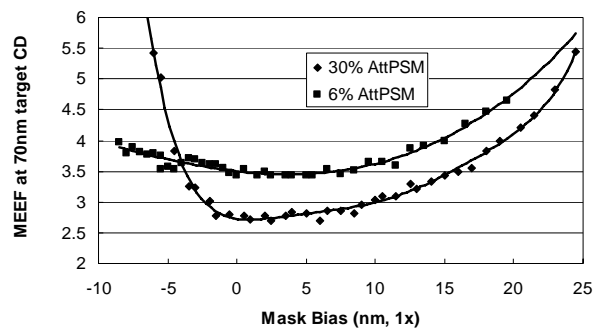


Figure-1: Prolith simulation of MEEF for 30% AttPSM vs. 6% AttPSM. (115nm CH pitch, 70nm CH target CD on wafer, 1.35NA, Quasar 30-deg. opening angle, 0.93-0.69 sigma outer-inner)

Inverse lithography (IL) defines an objective function in such a way the target intensity of the dark region is set to zero and the target intensity of the clear region is set to  $I_{max}$ , where  $I_{max}$  is the peak intensity taken from the dense array's intensity measurement [5]. Pixel optimization based on this objective function definition tries to achieve uniformity for all patterns such that all patterns attain nearly the same peak intensity while keeping the background intensity very close to zero. This leads to a situation where all patterns look similar in terms of intensity profiles, thereby resulting in better overlaps for common process windows. Since this optimization process tries to keep the background intensity as low as possible, it has an effect of side-lobe printing suppression through SRAF placements (Figure-2). In many cases, we observed that the SRAF placements that resulted from this optimization process tend to be rather counter-intuitive from a perspective of straightforward rule-based SRAF placement. Given IL's ability to automatically generate necessary SRAF patterns on the mask without chrome, mask making becomes less complex, and it is no longer necessary to place chrome in critical region between contacts in anticipation of possible side-lobe printing. For non-critical region which is significant away from any target features, use of chrome would be still necessary (Figure-3).

For converted clips of several 100 CH, we can calculate the process variation band histograms and MEEF for all edges using a litho rule checker such as OPC Verify. This was done for several 100 IL conversions of the clip shown in Figure 2, and the final result indicated that on average the 30% AttPSM had slightly larger process window and lower MEEF, at dense pitches, than 6% AttPSM. Figure 4 shows IL-conversion results for the same layout clip with 6% AttPSM and 30% AttPSM. SRAF's are placed at similar spots in the both cases, but SRAF's sizes tend to be larger in the 30% case in order to suppress background/side-

lobe printing, which is much more pervasive in the case of 30% AttPSM.

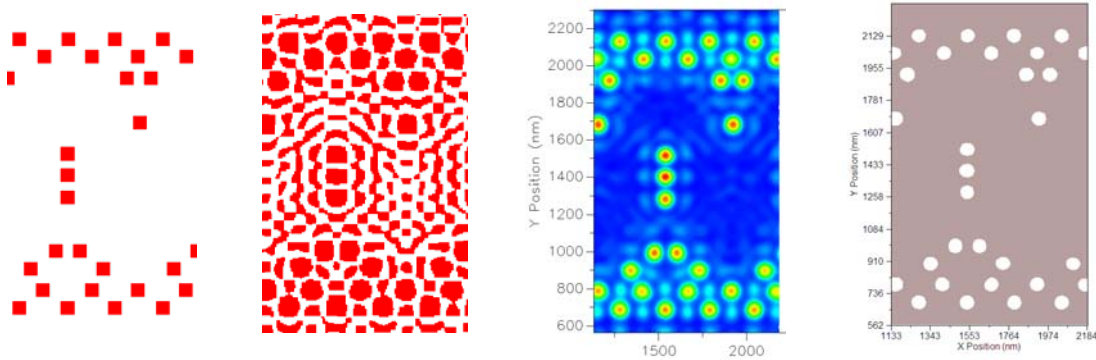


Figure-2: From left to right: (1) Target GDS layer (densest pitch 116nm in CH triplet) (2) IL solution for 30% AttPSM and Quasar illumination at 1.35NA (3) Image intensity in resist calculated by Prolith from the IL GDS in (2) and (4) Resist contour calculated by Prolith from the image intensity in resist. Note that no side-lobe printing occurs for the IL solution that does not contain any Cr borders.

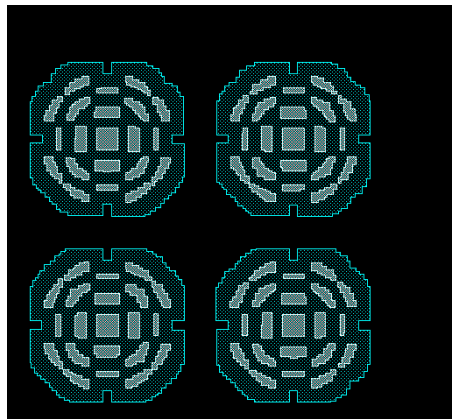


Figure-3: regional solution for 65nm CH at 800nm pitch. The fully dark area is covered by Cr. The dotted region is 30% AttPSM, and the light grey region corresponds to Qz.

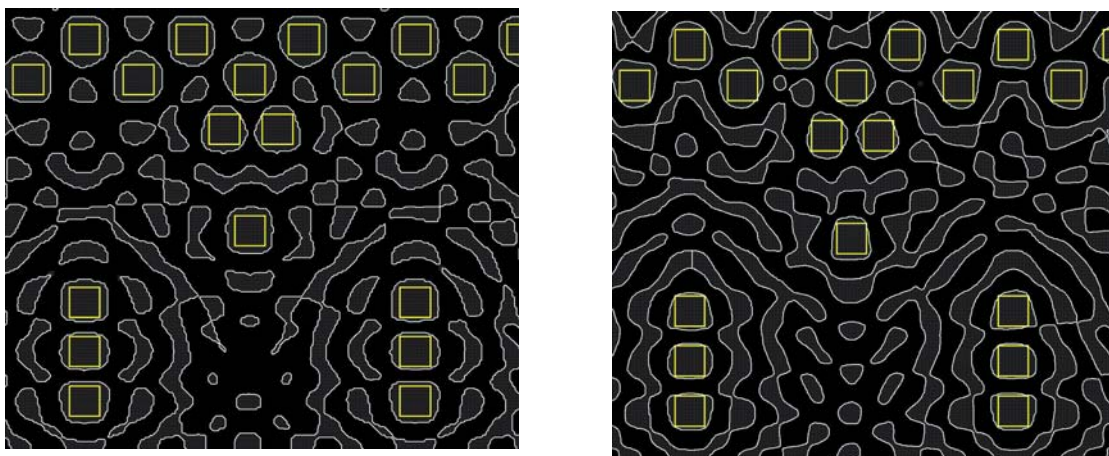


Figure-4: IL-converted results with 6% AttPSM (left) and 30% AttPSM (right). The solid-line rectangles are the targets. The dotted regions are IL-converted shapes. SRAF's are placed at similar spots in the both cases, but SRAF sizes tend to be larger in the 30% case.

### 3. EXPERIMENTAL DATA

#### 3.1 LAYOUT PATTERNS

We used the generic clip with 70nm target CD and with multiple pitches for a variety of configurations including CH on a line, CH orthogonal arrays, CH skewed arrays, CH doublets, CH triplets, and Random clip (repeated 5 times for averaging). Figure-5 shows the IL conversion results for some of these configurations. Dense CH arrays at multiple CD's and pitches were also repeated over the mask in 5 by 7 field positions for study of mask and wafer uniformity,

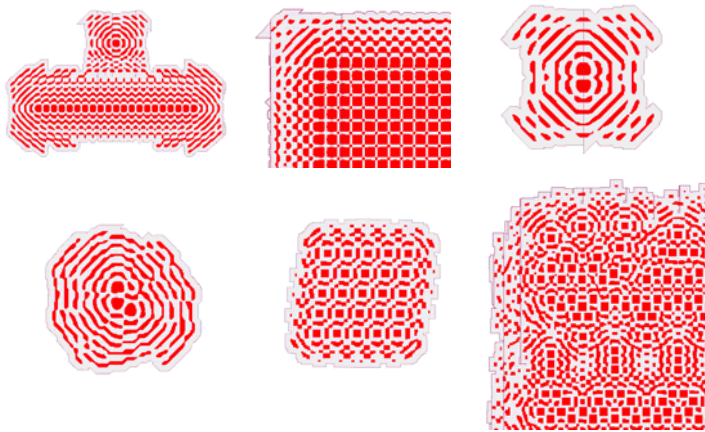


Figure-5: Patterns used for 30% AttPSM. Solid Red = Qz, dotted = 30% AttPSM, the area outside the dotted region is covered with Cr for background suppression

#### 3.2 MASK MAKING AND QUALITY

IL tends to generate a large number of SRAF's for 30% AttPSM, and some of them could be very small to such a degree that the mask patterning process cannot resolve them. For a 6% AttPSM, we have reported before that the patterning limit for a 6% AttPSM mask is set by the area of the AF, and became problematic when the area of the AF was less than  $2000 \text{ nm}^2$  at 1x (see reference 2). Figure-6 shows the overlay of an IL result and real mask for 30% AttPSM. Based on this we determined that a) those SRAF's with the area smaller than  $740 \text{ nm}^2$  disappear in the mask writing process (missing slots), and b) those SRAF's with the area smaller than  $900 \text{ nm}^2$  (and greater than  $740 \text{ nm}^2$ ) may not completely disappear but get significantly dimmer (marginal slots). We observed similar area constraints for 6% AttPSM Hence the maskmaking of the small AF between 6% and 30% AttPSM has similar area limitations. Also, since the AF for 30% AttPSM tend to be larger than for 6% AttPSM, the patterning of AF should even be less problematic.

We also measured the CD uniformity (CDU) of dense CH on the 30% AttPSM mask (Figure-7), and found similar mask uniformity as for 6% AttPSM. In combination with the lower MEEF for 30% AttPSM, this implies that a better uniformity on wafer should be attainable. Other factors that can affect wafer CD uniformity are mask transmission and phase. These were measured on a similar grid as the mask CD uniformity. The average phase was 179.4 degrees, with a range of 3.7 degrees over the mask. The transmission was 31.0%, with a range of 0.3% over the mask. All these measurements indicate that the quality of the 30% AttPSM was very similar to that of a 6% AttPSM. The Cr layer on the 30% AttPSM was present but not inspected, as its edges were always far from main feature edges.

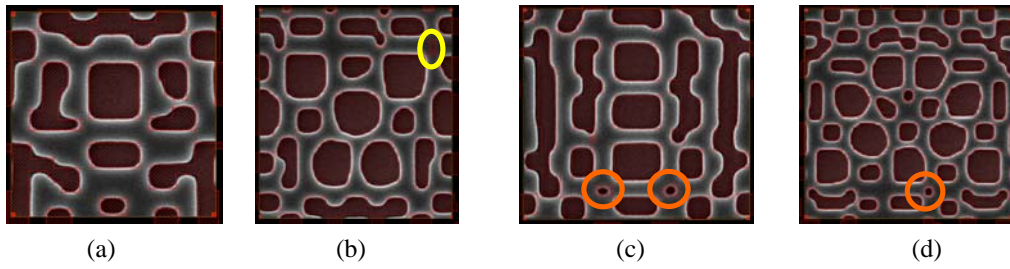


Figure-6: mask writing qualification – (a) clean case, (b) missing slot, and (c), (d) marginal slots

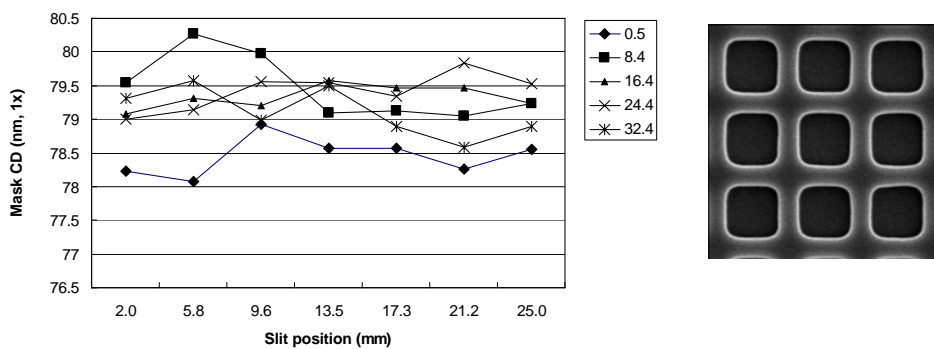


Figure-7: Measured CD evolution over the mask of a 80nm CH CD at 116nm CH pitch (30% AttPSM). The horizontal axis is the position on mask, and the lines represent different Y positions. CD is the average CD of a H and V CD measurement over a single CH. The CD range = 2.2nm at 1x, which is similar as seen on 6% AttPSM for an identical measurement.

### 3.3 VALIDATION BY AIMS-45

The IL technology implemented in Mentor Graphics pixbar<sup>TM</sup> software uses the SOCS [7] technique for optical image computation. The SOCS kernels are derived from TCC and can account for the physical effects that can be incorporated in TCC. Because of the extensive use of optical image analysis by the IL technology, it is of significant benefit if there is a measure to observe the image intensities in resist directly without the intermediate steps of doing multiple reticle SEM measurements followed by extensive electromagnetic field simulation. The AIMS<sup>TM</sup>-45, when used in scanner mode, can emulate the image intensity as seen in resist on wafer at scanner illumination conditions [6]. Hendrickx, et al. conducted detailed investigation using AIMS-45 on IL conversion results for Quasar illumination with 6% as well as 30% AttPSM background [3]. The benefit of using AIMS-45 is that the measurement occurs at scanner illumination conditions and through the actual mask. As discussed in reference 3, the measurement results from AIMS-45 correlated well to wafer data, but had the benefit of being easier to capture and average than SEM data.

Figure-8 shows AIMS-45 image of the random CH clip with 30% AttPSM. Maximal intensity inside CH was targeted at 0.60 by IL conversion. AIMS-45 measurement shows that this intensity level is achieved, and also that the background intensity is well suppressed by the placement of AF. Figure 9 shows the EL and DOF extracted from the AIMS-45 image intensities for a 30% AttPSM mask along with a 6% AttPSM. Here we see that the 30% AttPSM has slightly larger process windows than 6%, as was also seen in simulations using OPC Verify.

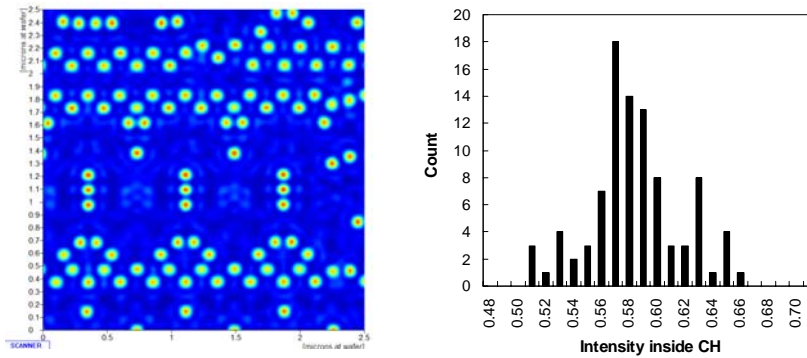


Figure-8: AIMS-45 image of the random CH clip after IL conversion with 30% AttPSM (left) and the distribution of the maximal intensities measured in each CH (right)

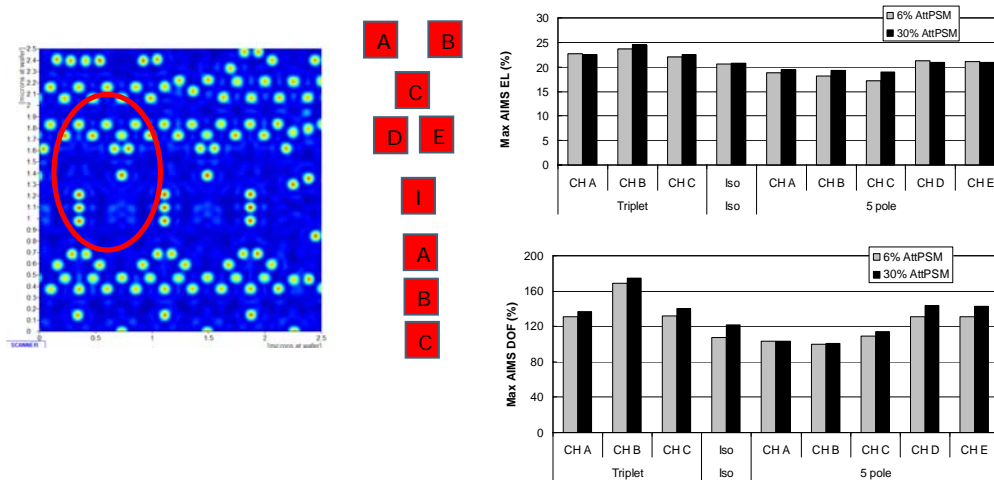


Figure-9: AIMS-45 measurement of process window; the layout clip (left), and the schematics of CH for the measurement (center), and EL (right/top) and DOF (right/bottom). The graph top right has the maximal EL from the AIMS measurement for the 30% AttPSM, as well as a comparable clip for 6% AttPSM. The graph bottom left has the same comparison, but now for DOF.

Figure-10 shows IL conversion results for regular CH array through pitch as well as AIMS-45 image intensities. At every pitch, we measured the maximal array inside the main CH, and the intensities along the horizontal and diagonal direction between the CH. The intensity inside the main CH reaches the target level of 0.6 for almost all pitches. The intensity threshold at which the main CH is at the required target CD is around 0.3. The measurement also shows that the background intensities are well controlled, since the intensity between the CH along the horizontal and diagonal orientation stays well below the 0.3 intensity threshold. The AIMS-45 measurement for the same CH array through pitch shows that process window maintains the maximum DOF greater than 100nm and EL greater than 15% EL above 190nm pitch (Figure-11). We have also measured CD uniformity at 116nm pitch on AIMS-45 on 6% and 30% AttPSM (Figure-12). For both 6% and 30% AttPSM, we used 80nm CH CD on reticle to generate 65nm CH CD on wafer. We have found the 30% AttPSM to give 30% smaller CD range on wafer in AIMS45 CDU test.

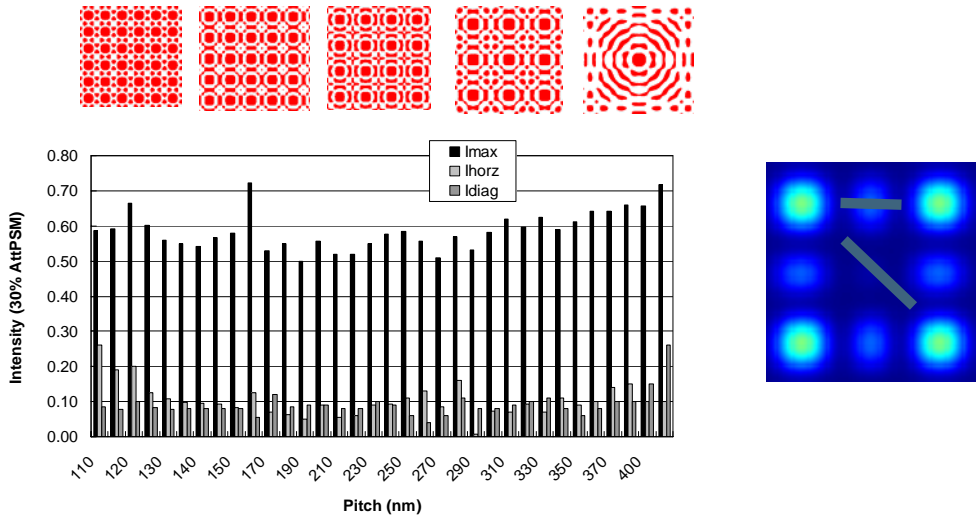


Figure-10: (top) converted patterns for regular CH array through pitch, (bottom) intensities measured inside the main CH ( $I_{max}$ ) and along the horizontal ( $I_{horz}$ ) and diagonal ( $I_{diag}$ ) orientation between the CH.

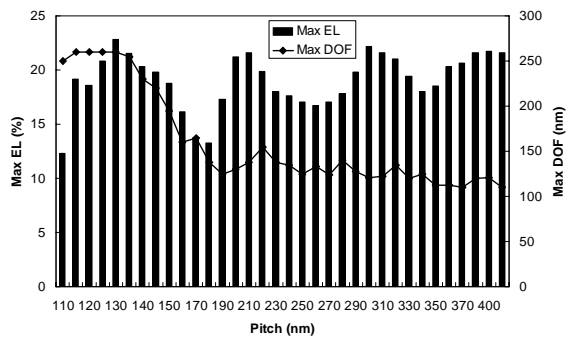


Figure-11: AIMS-45 process window parameters for 30% AttPSM regular CH arrays through pitch. Left axis (bars): Max EL through pitch. Right axis (line): Max DOF through pitch

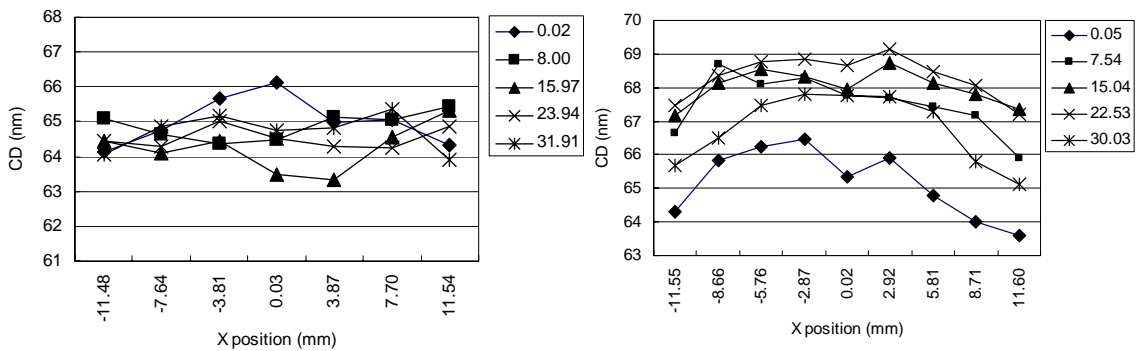


Figure-12: Intrafield CDU of 65nm CH at 116nm pitch for 30% (left) and 6% AttPSM (right) as measured by AIMS-45. The X-axis is the X position coordinate on the mask, the different lines are for different Y positions on the mask. Each point is the average CD of 9 CH in that particular location.

### 4.3 WAFER VALIDATION

We exposed the IL-converted patterns with ASML XT:1900i (1.35NA, Quasar 0.93-0.69 illumination). A first inspection on wafer confirmed the simulations and AIMS-45 measurements, with good background printability control and pattern fidelity for the different geometries (Figure-13). MEEF was measured for pitches 116, 118 and 120nm on wafer for a 6% and 30% AttPSM (Figure-14). The wafer CD is 70nm with the mask bias of 16nm. MEEF was then measured at 3 dense pitches near the resolution limit and was about 30% lower for 30% AttPSM, and confirmed the tendency seen in simulation (Figure 1).

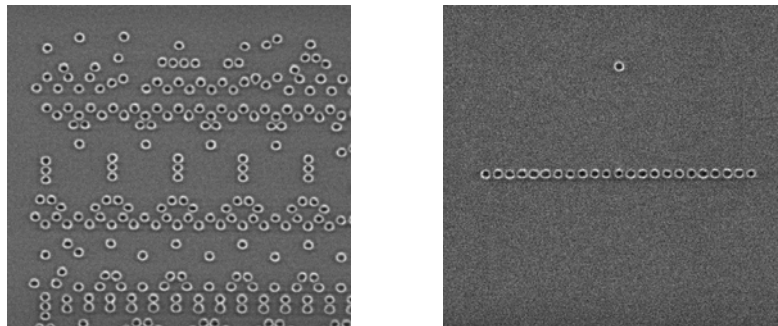


Figure-13: The image of IL-converted patterns on wafer; random CH (left) and CH on a line at 105nm pitch (right); exposed with ASML XT:1900i (1.35NA, Quasar 0.93-0.69 illumination)

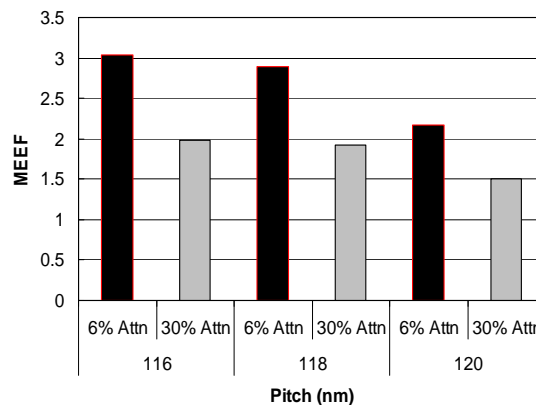


Figure-14: CH MEEF near the resolution limit for 6% AttPSM and 30% AttPSM

Since MEEF for a 30% AttPSM is lower, and the mask is of similar quality as a 6% AttPSM, the intrafield CDU should also be better for 30% AttPSM. The Intra-field CDU was measured for 116nm pitch on wafer for a 6% and 30% AttPSM when the masks were exposed back-to-back (Figure-15). The CD is 70nm and the mask bias is 15nm. The 30% AttPSM case shows significant reduction in measured CD over the 6% case.

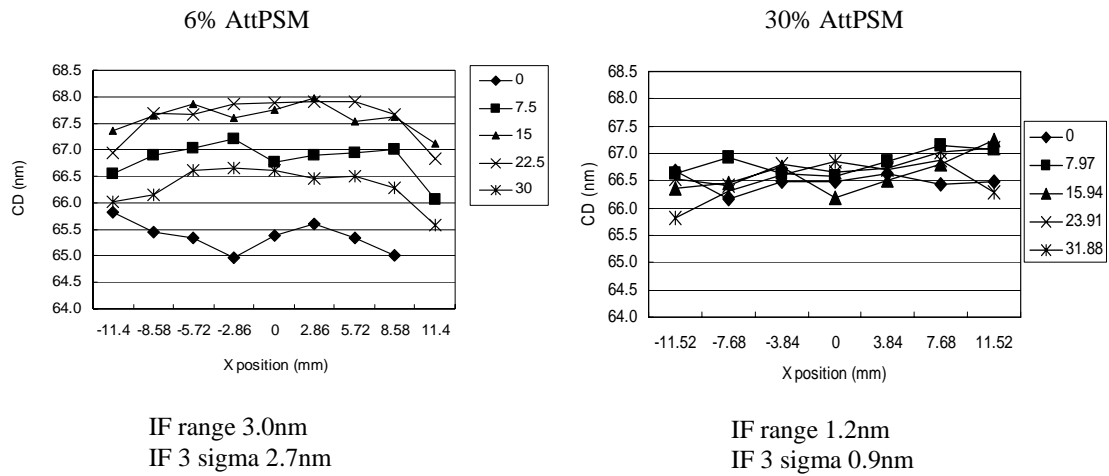


Figure-15: CD uniformity measurements; 6% AttPSM (left) and 30% AttPSM (right)

One issue was noticed on the 30% AttPSM that needs further optimization. Even though the mask phase was well on target for the large phase measurement targets, we noticed some asymmetry in the Bossung plots at semi-dense to isolated pitches. Such effects have been seen before in phase shift masks where the phase shift is attained by etching into Qz, such as Chromeless Phase Lithography (CPL) masks. This effect is not seen in traditional 6% AttPSM MoSi blanks, where the phase shift is obtained by an etch into MoSi. Our 30% AttPSM used a thin MoSi layer, and partially etched into Qz to attain 180 degree phase shift. Since narrow Qz features control phase less effectively than large Qz features, this can induce a phase error for narrow Qz features when large feature have the correct phase. Tilted Bossung occur. For CPL masks, the Bossung tilt could be solved by etching slightly deeper into the Qz. Figure-16 shows the measured Bossung plots of 400 and 280nm pitch CH for the IL-converted patterns. Bossung tilt is visible, and was confirmed by AIMS measurement and rigorous simulation. Corresponding patterns from 6% AttPSM did not show tilt. We anticipate that it should be possible to solve the issue by optimizing the Qz etch depth, as was done for CPL.

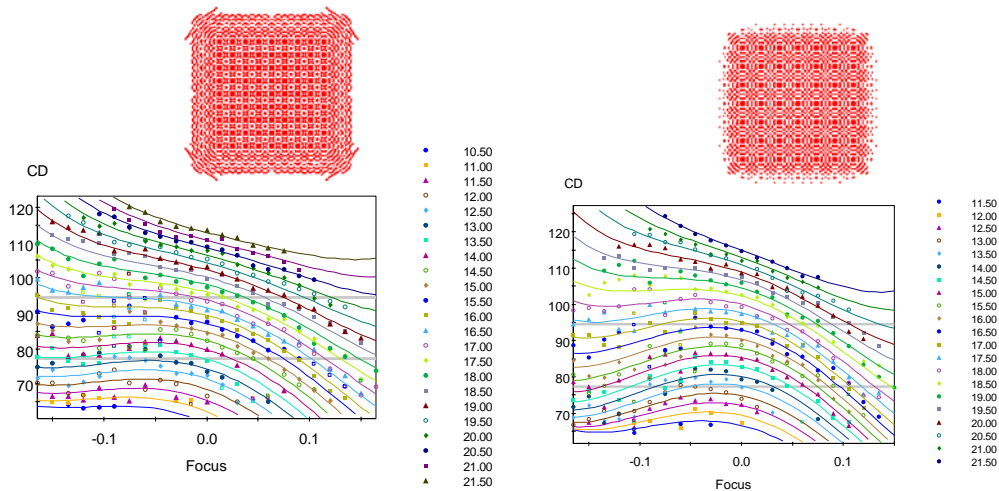


Figure-16: Bossung plot for the IL-converted patterns for 280nm pitch (left) and for 400nm pitch (right) on the 30% AttPSM.

#### 4. PRACTICAL TECHNIQUES FOR MRC

The pixel inversion generates polygons that comprise a number of small edges with arbitrary angles. Those arbitrary mask shapes are problematic for mask writing purposes in terms of both mask writing time as well as mask drawing accuracy due to small figures. Enforcement of mask manufacturing rules (MRC), on such inverse lithography results is a complex problem. There are several specific MRC rules to enforce as follows:

- 1) Minimum fragment length
- 2) Minimum width of SRAF's
- 3) Minimum spacing among SRAF's
- 4) Minimum spacing between SRAF's and the main target features
- 5) Minimum SRAF area

These MRC requirements need to be met under the following underlying conditions:

- a) Only orthogonal and/or 45-degree edges must be used to construct MRC-compliant shapes
- b) The resultant shapes should not be too different from the original IL shapes
- c) The MRC compliance should not be achieved at the cost of too much polygon deletion

Except for the condition of a), these underlying conditions are somewhat ambiguous due to the trade-offs that need to be taken into account when dealing with conflicting conditions. For example, it may be possible to achieve MRC compliance by deleting some polygons, but deleting large SRAF's would compromise the imaging qualities. Some of SRAF's may be only slightly narrower than the required minimum width, and deleting them may impair the imaging qualities greatly. It may be possible to keep such SRAF's by making them slightly wider, but such manipulation may cause additional spacing violations. These types of conflicting situations can happen in various ways, and there is no trivial solution to deal with them.

To handle these issues, we employ practical techniques based on the geometrical simplification procedure which is briefly described in [4]. The geometrical simplification approximates the raw pixel inversion results using orthogonal angles and/or *octagonal* angles, i.e. the orthogonal angles plus 45-degree angles. The basic algorithm of the simplification is as follows: 1) group the raw edges together based on the angle approximation, 2) compute the simplified edge placement for each of the edge groups, and 3) compute the intersections for the simplified edges and close the polygon loop (Figure-17).

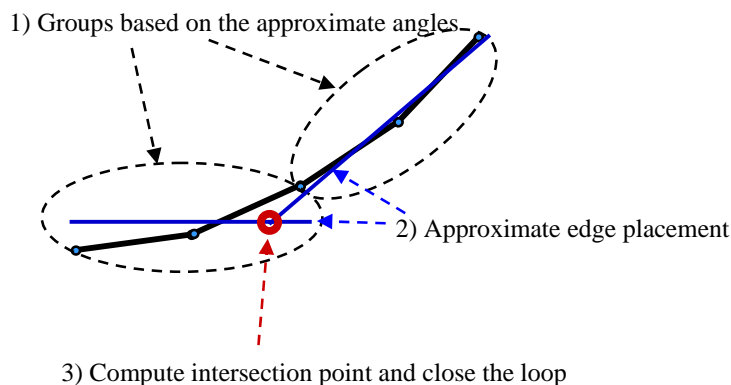


Figure-17: illustration of the simplification algorithm (the black solid lines are the raw edges from the pixel inversion)

While the geometrical simplification helps improve the manufacturability to some extent, it does not ensure the full MRC compliance. Our approach to the MRC-compliance is to use the geometrical simplification as the central algorithmic hub to take care of the various issues. We describe our techniques to actually device

mechanisms to address these issues in the following sub-sections:

a) The minimum fragment-length enforcement

The minimum fragment-length enforcement is a requirement that there should not be two or more consecutive edges with the length shorter than the specified minimum fragment length. It is considered MRC-compliant, if it's just one short edge sandwiched by two long edges (Figure-18).

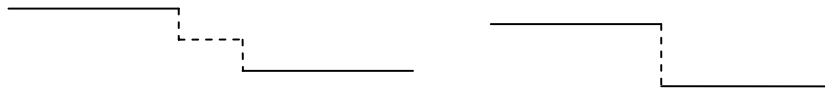


Figure-18: An example of minimum fragment length violation (left), and (b) an example of minimum fragment length compliance despite the presence of a short edge (right). Solid-lines are long edges, and dashed-lines represent short edges

In our approach, the fragment-length enforcement is a variation of the geometrical simplification process. We transform the geometry shapes in such a way that the simplification of the transformed shapes result in improved fragment-length compliance. For the purpose of such geometry transformation, we use a technique called middle-point conversion to deal with these short edges. The basic idea is to (a) compute the middle point for each of these short edges, (b) connect them together, and (c) perform the geometrical simplification on the converted shapes (Figure-19).

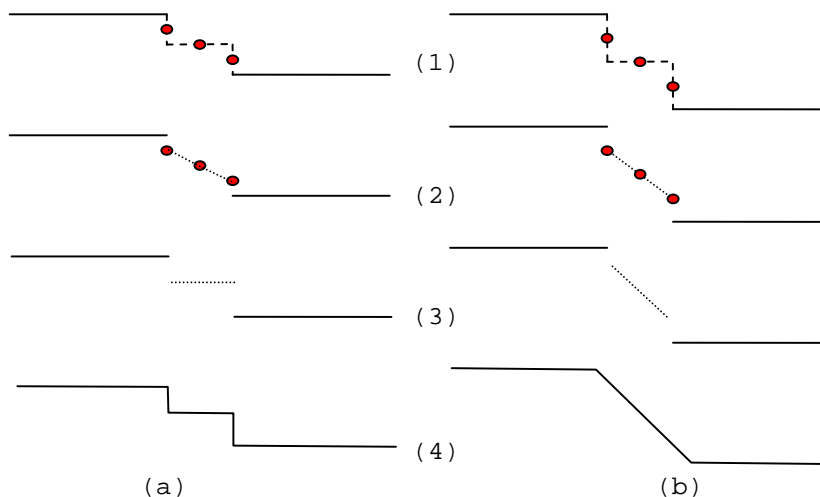


Figure-19 Illustration of the middle-point conversion scheme for geometrical configurations with short stair-steps in the middle; in the case of the left-column (a), (1) the middle points are computed for the short edges, (2) a line is drawn through the middle points, (3) an approximate line is drawn based on the angle group (horizontal in this case), and (4) the intersections are calculated and the lines are connected; in the case of the right-column (b), the approximate angle in (3) is 45-degree, and the 45-degree line is used to form the final shape

b) The minimum space/width enforcement

The minimum fragment-length enforcement does not concern the minimum space/width conditions. There has to be an additional mechanism to enforce these spacing-related constraints. Given the complexity of the possible combinations of various geometrical configurations, there is no easy way to even determine what

the right result should be like. For example, some SRAF's may be only slightly narrower than the required minimum width. It is not desirable to simply delete such polygons, because a) it tends to lead to the situation where too much polygons are deleted, and b) there may be negative impact on the imaging if too much polygons are deleted. It may be possible to make such slightly narrow SRAF's slightly wider to satisfy the minimum width requirement. However, whenever any polygons are made wider, they can cause spacing violations with nearby polygons. To deal with such difficulties, we employ an iterative scheme. The basic idea of this scheme is illustrated in Figure-20.

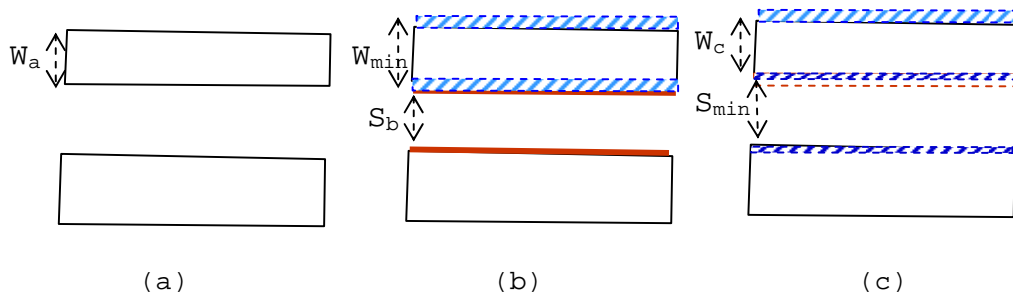


Figure-20: Illustration of the iterative scheme to correct spacing constraints; (a) shows a pair of rectangles with the one at the top has the width ( $W_a$ ) that is smaller than the minimum required width ( $W_{min}$ ), (b) shows the widened polygon shape of the top rectangle to satisfy the minimum width requirement, but it also causes a spacing violation ( $S_b$ ) with the rectangle at the bottom, and (c) shows a correction with regard to the spacing violation, which could cause the width ( $W_c$ ) of the top rectangle to be smaller again, thereby making it necessary to perform the width correction step again. The whole process is repeated several times this way.

#### c) The minimum area enforcement

Similarly to the handling of SRAF's with the width that is slightly narrower than the required minimum width, it is not desirable to simply delete those SRAF's whose area is slightly smaller than the required minimum area. Our approach is to compute the area for each SRAF and if the area is smaller than, say, 75% of the minimum area, then delete them. If the area is between 75% and 100% of the minimum area, then we compute the extent of the SRAF and adjust it so that it will attain the minimum area. If the area is greater than 100% of the minimum area, it's kept as it is.

#### d) Overall flow and limitations of the approach

Each of these individual components of the MRC solution can cause additional MRC violations on other categories. We employ an iterative scheme on the overall flow that involves these component solutions as follows:

- 1) Perform the initial octagonal geometrical simplification on the raw IL result
- 2) Widen the narrow shapes
- 3) Widen the narrow spaces
- 4) Perform the fragment-length enforcement
- 5) Perform the minimum area enforcement
- 6) Check if there are MRC-violations remaining, and if yes, go back to 2)

Figure 21 shows some snapshots of the MRC process. The approach we employ is an assortment of various practical techniques as described above. It is possible that the final outcome of this MRC process is not necessarily fully satisfactory due to the complexity of the problem. In some cases, after some attempts to keep narrow SRAF shapes, the software system still may not find enough space to widen the shapes, and

they would have to be removed in the end. Another issue is that, although this approach tries to preserve the original IL-converted shapes as much as possible, it is still possible that geometry modifications for MRC impair the imaging qualities achieved by IL-conversion. However, we also would like to point out i) dose optimization plays an important role, as higher dosage generally results in narrower SRAF shapes and lower dosage results in wider SRAF's shapes, which can have a major impact on MRC, ii) it may also be necessary to tune the optical system with the SRAF generation in mind, so that the selection of the optical system along with the dosage are friendlier to SRAF generation and OPC, and iii) it is still highly important to verify/validate the final results with imaging analysis tools. A possible flow, as an example of this overall consideration, would be to (1) extract parameters that are necessary to run IL and OPC, such as  $I_{\max}/I_{\min}$  and resist threshold, from the tightest pitch array for various combinations of source illumination and dosage conditions, (2) apply IL, MRC and OPC using the extracted parameters from (1) on a sample layout clip which contains various pitches in various configurations, and (3) measure common process windows for the results of (2) to pick the best combination.

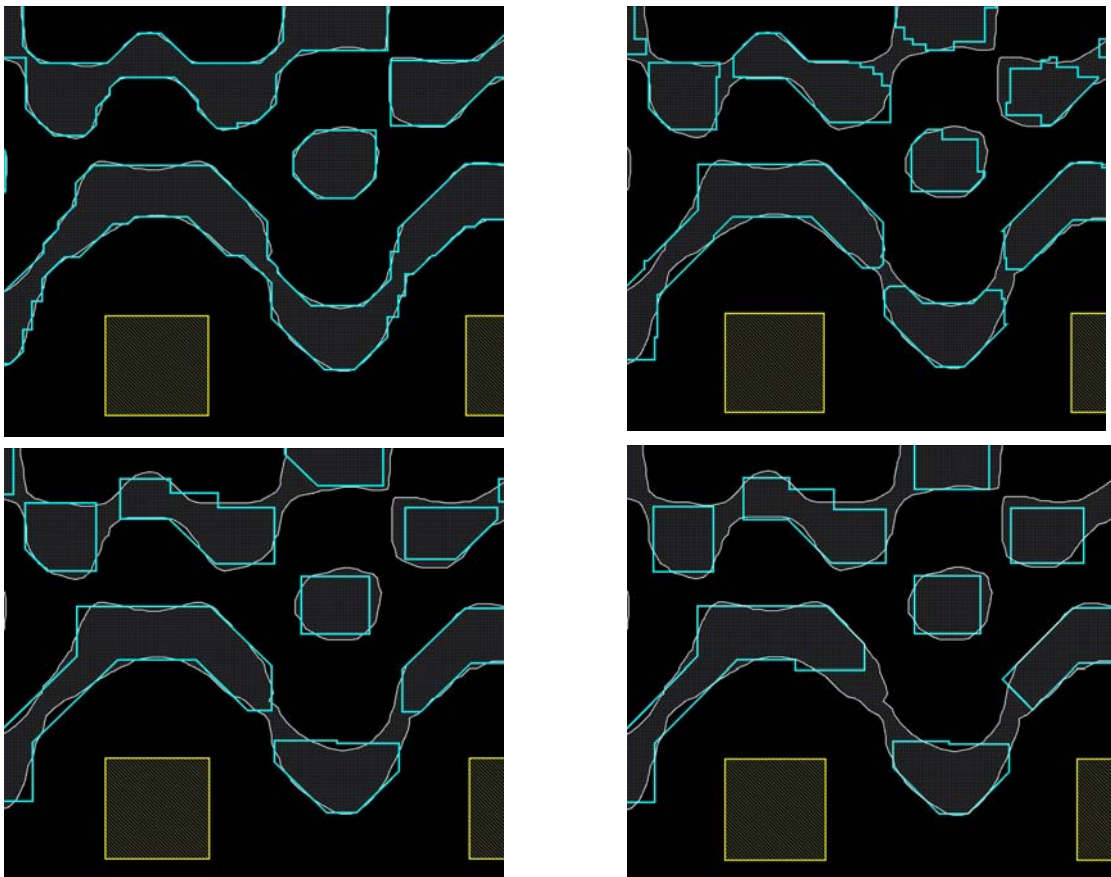


Figure-21: MRC processing snap shots : the first one on the top left shows the raw IL-converted result (dotted regions) overlaid with the initial simplification result (solid-lines) along with the target shapes (shaded regions), the top right shows the first iteration result after the step-3) (solid-lines), the bottom left shows the first iteration result after the step-4) (solid-lines), and the bottom right shows the final result (solid-lines) after all iterations.

## 5. SUMMARY

We applied the inverse lithography technique to automatically generate SRAF's for the 30% AttPSM

background case, and compared the results the 6% AttPSM case. We have confirmed that the inverse lithography generates SRAF patterns to suppress the side-lobe printing which could be prevalent in the case of 30% AttPSM due to the fact that the default background intensity could be higher than the resist threshold. We also have confirmed the 30% AttPSM's MEEF is lower than that of the 6% case. For maskmaking, due to the use of SRAF's for sidelobe suppression, the need for Cr is limited to regions far from the main CH, which reduces the number of critical layers from 2 to 1 for high transmission masks. Compared to 6% AttPSM, the 30% had similar uniformity of CD, phase, and transmission, and gave smaller interfiled CD uniformity when tested back-to-back with a 6% AttPSM. One parameter that remains to be optimized is the optimal mask etch depth, to reduce the impact of possible reticle 3D effects on process window symmetry. As such, inverse lithography can be seen as an enabler for high-transmission reticles.

We provided the description of the practical algorithmic techniques to handle MRC constraints to make the resultant shapes manufacturable, while keeping the shapes as close as possible to the raw results to preserve the imaging qualities achieved by the inverse lithography. Limitations of the MRC approach were also discussed.

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