

Characterizing the imaging performance of Flash Memory masks using AIMSTM

^aEelco van Setten, ^aOnno Wismans, ^aKees Grim, ^aJo Finders, ^bMircea Dusa,

^cRobert Birkner, ^cRigo Richter, ^cThomas Scherübl

^aASML Netherlands B.V., De Run 6501, 5504 DR Veldhoven, The Netherlands

^bASML TDC, 4800 Great America Parkway – Suite 500, Santa Clara, CA 95054, USA

^cCarl Zeiss SMS GmbH, 07740 Jena, Germany

ABSTRACT

Flash memory has become one of the most important segments of the semiconductor industry in recent years. Flash memory is also an important driver of the lithography roadmap, with its dramatic acceleration in dimensional shrink, pushing for ever smaller feature sizes. The introduction of the XT:1700Fi and XT:1900Gi have brought the 45nm node and below within reach for memory makers. At these feature sizes mask topology and the material properties of the film stack on the mask play an important role on imaging performance. Furthermore, the break up of the array pitch regularity in the NAND-type flash memory cell by two thick wordlines and a central space, leads to feature-center placement (overlay) errors, that are inherent to the design. An integral optimization approach is needed to mitigate these effects and to control both the CD and placement errors tightly.

In this paper we will present the results of aerial image measurements on mask level of a NAND-Flash Memory Gate layer using AIMSTM 45-193i. Various imaging relevant parameters, such as MEEF, EL, DoF and placement errors are measured for different mask absorber materials for features sizes ranging from 39nm half pitch to 41nm half pitch design rule on wafer level. The AIMSTM measurements are compared to experimental results obtained with a XT:1900Gi hyper-NA immersion system. Mask optimization strategies are sought to increase Depth of Focus and minimize feature-center placement errors.

Keywords: AIMS , NAND-Flash, hyper-NA, immersion lithography, polarization

1. Introduction

Flash memory has become one of the most important segments of the semiconductor industry in recent years. Flash memory is also an important driver of the lithography roadmap, with its dramatic acceleration in dimensional shrink, pushing for ever smaller feature sizes. The latest generation of hyper-NA immersion tools has brought the 40nm node within reach for memory makers (Figure 1). At these feature sizes mask topology and the material properties of the film stack on the mask play an important role on imaging performance¹. Polarization has become an integral part of the illumination scheme and the film stack on the mask can no longer be regarded as infinitely thin, making rigorous simulations necessary for accurate process window and OPC simulations. However, run-time and the memory required by lithographic simulators increases tremendously when 3D mask effects are incorporated in the simulation of 2D structures, making simulations of complete design clips for most simulators impossible.

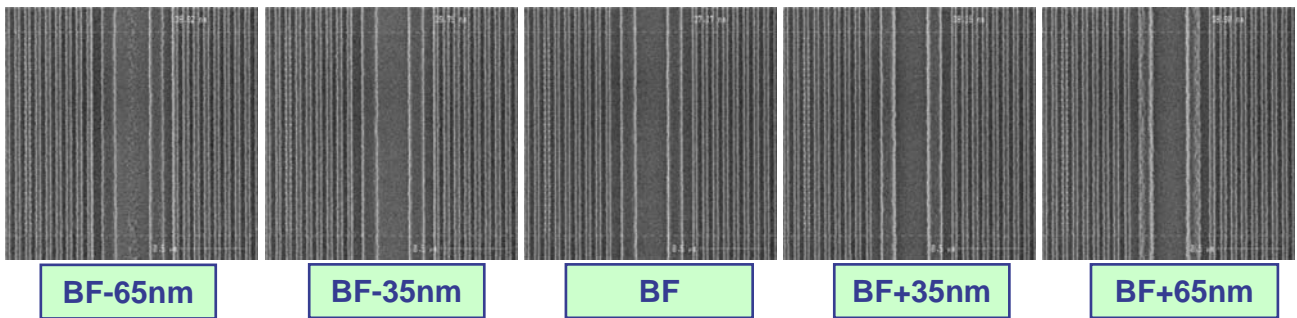


Figure 1 NAND-type flash memory gate layer with 39nm half pitch design rule exposed on an XT:1900Gi immersion scanner. Good image integrity is observed over 130nm focus range.

The NAND-type flash memory cell (Figure 2) is organized in separate modules (pages) containing 32 wordline transistors (wordline poly gates) with 2 select transistors (select poly gates) and with one source and drain contact for the entire 32 page module. The array-core zone consisting of 32 equal line-spaces allows for aggressive low-k1 imaging with extreme off-axis illumination. However, the presence of the two mirrored SG lines and the SG-SG gap, break up the array pitch regularity and create a discontinuity in layout topology. Dusa et al² showed that this discontinuity introduces an asymmetry in the near field diffracted intensity under the left and right edges of the SG line, as well as under the adjacent next 4 to 5 wordlines (see Figure 3). The lithographic performance of the mask layout is affected by this cross-coupling effect, which induces feature-center placement errors through dose and focus.

To study these effects at mask level, and to discriminate between the mask and the scanner, a test mask has been measured using AIMSTM 45-193i³. Exposures were performed with an XT:1900Gi hyper-NA exposure tool. The test mask contains NAND-type flash memory clips, regular L/S gratings and MEEF modules at multiple features sizes patterned in MoSi, and MoSi covered with a chrome layer. In this paper we will present the results of the aerial image measurements on mask level and compare them to CD-SEM measurements from the exposures on wafer level. In a number of cases these measurements are also compared to simulations. We will focus on MEEF, EL, DoF and feature-center placement errors.

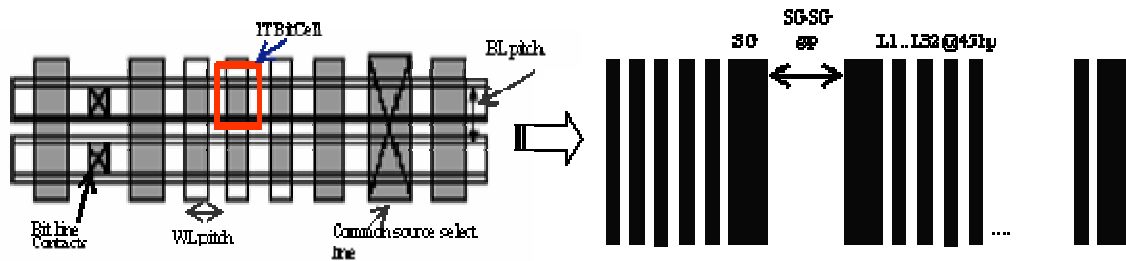


Figure 2 Left: Flash memory core layout for critical layers: poly wordline and interconnect bitline and contacts. Layout simplicity with unidirectional regularity is noticeable. Right: Characteristic topology of poly wordline layout with line/space regularity broken by SG and SG-SG gap. Design rule defines SG and SG-SG gap dimensions as multiple integers of half pitch.

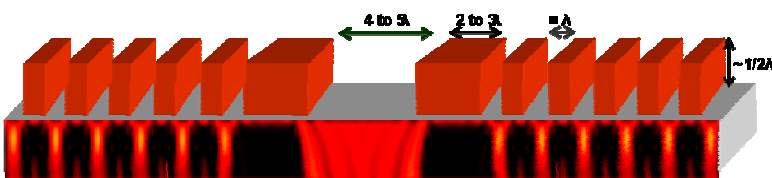


Figure 3 Scattered near field diffracted intensity for TE-polarized illumination from flash wordline mask pattern. An asymmetry under the left and right edges of the SG line and adjacent wordlines is visible.

2. Experimental conditions

All exposures and measurements were done with a test mask from AMTC -Toppan. The film stack of the mask consists of a 680 Å MoSi layer covered by a 580 Å chrome layer. The MoSi-features (after patterning) have an average phase shift of 180° and transmission of 6.15%. The binary structures are patterned in the thick MoSi + Cr stack as opposed to traditional Chrome-On-Glass (COG) binary masks, which do not have a MoSi layer between the Cr top and the glass substrate. In this paper, the term ‘Binary’ will be used for the ternary stack as described above, while ‘Attenuated’ refers to the 6.15% transmission of the MoSi-features. A schematic representation of the mask stack on our test reticle, and the reticle itself can be found in Figure 4 below.

The mask has been measured extensively with an AIMS™ 45-193i aerial image measurement system from Zeiss. The AIMS™ 45-193i has a maximum scanner equivalent NA of 1.4, which enables the emulation of the latest generation of hyper-NA immersion scanners. Furthermore it is possible to use polarization and multiple off-axis illumination modes, equivalent to scanner illumination modes. The aerial image measurements were done at NA = 1.35 and $\sigma = 0.78 / 0.98$ Dipole X illumination with 35° opening angle and linearly polarized light (Y-polarized) in ‘Scanner Mode’⁴ to capture the vector effects associated with hyper-NA imaging. In the “Scanner mode” the aerial image in resist will be generated as a result of a combination of actual image measurements in the scalar mode (or “AIMS™ mode) and a Zeiss proprietary algorithm. Additionally, the user has to input the refractive index of the resist. In this work the refractive index was set to 1.7, which is equivalent to the refractive index of the photo resist used during the exposures.

The exposures were performed with an ASML XT:1900Gi hyper-NA exposure tool with a maximum NA of 1.35. The illumination conditions were optimized for 40nm half pitch using NA = 1.35 and $\sigma = 0.807 / 0.967$ Dipole X illumination with 35° opening angle and linearly polarized light (Y-polarized). The exposures were done on bare Si wafers coated with 93nm Brewer Science ARC93SR BARC, 95nm TOK TARFPi6001 resist and a 90nm JSR TCX041 top coat. All wafer measurements were carried out by CD SEM (Hitachi CG-4000).

The difference in sigma settings between the AIMS™ measurements and the exposures has been chosen on purpose to closely match the intensity profile of the scanner illumination source. The AIMS™ source can be regarded as top-hat illumination, whereas the scanner source has a more Gaussian intensity distribution. Furthermore, sigma-inner/ -outer on the scanner are defined as the radius where 10% / 90% of the total energy is encircled, whereas the top-hat sigma settings are the defined at the edges (0% / 100% of the encircled energy).

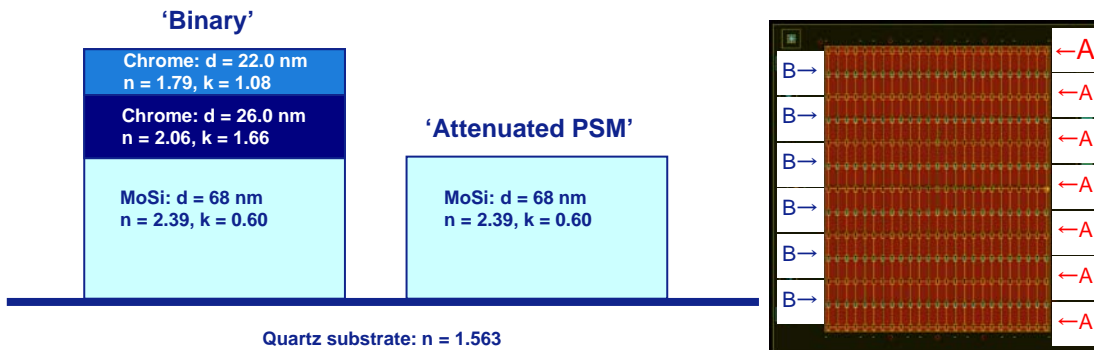


Figure 4 Left: Schematic representation of the mask stacks and their optical constants used in the simulations and experiments. Right: Test mask with alternating rows of attenuated (A) and binary (B) features.

3. Mask Error Enhancement Factor

In this section the Mask Error Enhancement Factor⁵ measurements with AIMS™ on mask level and CD-SEM on wafer level are compared to rigorous simulations. The MEEF has been studied for 2 different mask absorber materials by looking at fully dense (1:1) 1-D lines and spaces (L/S) gratings with 39, 40 and 41 nm feature sizes.

Figure 5 shows the MEEF measured with AIMS™ compared to rigorous ‘Image in resist’ simulations (Prolith 9.3.4.7) for 39, 40 and 41 nm dense L/S gratings. The simulations show that the MEEF is slightly larger for the attenuated features compared to the binary features in all cases. However this can not be supported by the AIMS™ measurements,

which show that the MEEF for binary and attenuated is equal within the test repro (approximately ± 0.2 nm/nm). In all cases there is quite a good agreement between the measured and simulated MEEF. The observed differences could be very well due to the fact that the 3D mask model used in the simulations is an idealized version of the real stack. Details like exact n and k values per layer, film thickness and side wall angle, which are correctly considered in the AIMSTM measurement, are often difficult or very time-consuming to determine experimentally, while they can have a significant impact on the outcome of the simulations. The side wall angle, for instance, can have a significant influence on the MEEF. We simulated a sensitivity in the order of 0.1 nm/nm MEEF change per degree side wall angle. Since the accuracy of a side wall angle measurement is typically around ± 2 degrees an uncertainty in MEEF of ± 0.2 nm/nm can be expected. We assumed a (constant) side wall angle of 86 degrees in the results presented here.

In Figure 5 also the MEEF measured by CD-SEM on the wafer is compared to full resist simulations using the measured illumination source shape (in contrary to the top-hat source shape used for the 'Image in resist' simulations). The simulated MEEF agrees again reasonably well with the measurements in all cases. The measured MEEF of the 41nm dense L/S is significantly lower than the simulations predict, which is in accordance with the AIMSTM measurements that also show a lower MEEF than expected based on simulations, especially for this case. From both the simulations and the CD-SEM and AIMSTM measurements it can be deduced that $\sim 70\%$ of the MEEF is determined by the optical properties of the mask, like the feature size and absorber material of the mask in combination with the used NA and illumination mode, while $\sim 30\%$ is determined by the chemistry (contrast) of the photo resist.

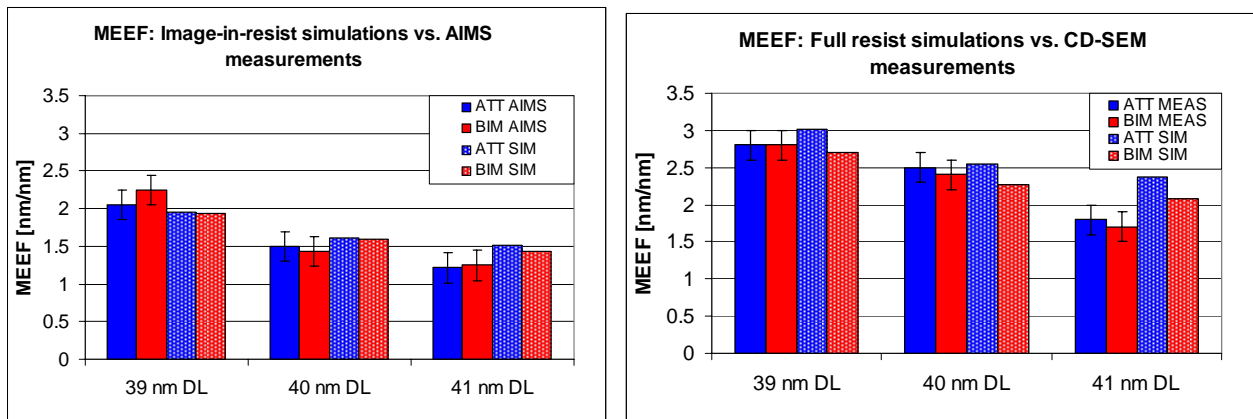


Figure 5 MEEF measurements versus simulations for 39, 40 and 41nm dense L/S gratings. Left: AIMSTM compared to image-in-resist simulations. Right: CD-SEM compared to full resist simulations.

4. NAND-type flash memory cell

In the next section the measurement results from NAND-type flash memory structures are presented. Various imaging parameters that are relevant for exposing the flash memory gate layer have been studied with the same test mask as described in section 2. Flash memory gate structures with 39 and 40 nm half pitch flash memory gate structures were exposed on an XT:1900Gi hyper-NA immersion system and measured with AIMSTM 45-193i aerial image measurement system.

4.1. Flash wordline mask pattern

Figure 6 shows the features from the flash wordline mask pattern that was evaluated in this study: The central space (SGSG), select gates (SG), wordline 1, 2 and 7, and the spaces between SG and WL1 (SP0) and between WL1 and WL2 (SP1). All 7 features were measured with AIMSTM on mask level and with CD-SEM on wafer level in resist. Wordline 7 is regarded as fully dense and is used as reference to print the gate layer on target. A basic OPC treatment has been applied using the thin mask approximation (Kirchhoff) and a lumped parameter resist model.

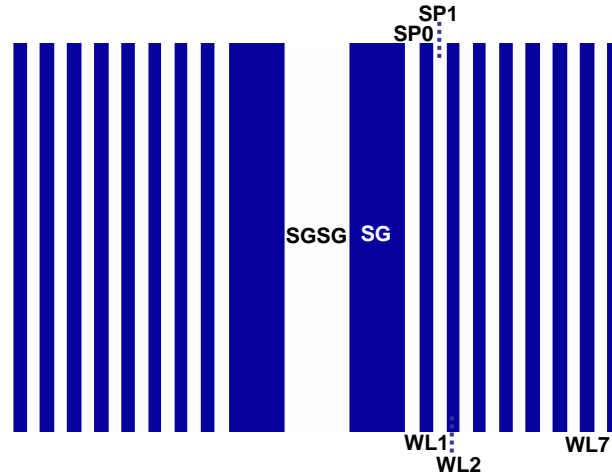


Figure 6 Features from the flash wordline mask pattern that were evaluated with AIMSTM and CD-SEM: Central space (SGSG), Select gates (SG), space between select gate and first wordline (SP0), wordline 1 (WL1), first space (SP1), second wordline (WL2) and the 7th wordline (WL7)

The test mask contains per feature size two designs with a different design rule for SP0, one of the most critical features in the gate layer. In the first design SP0 has a target CD which is equal to 1.5 times the design rule half pitch (e.g. $1.5 \times 40\text{nm} = 60\text{nm}$ space). In the second design the space has been increased to 2.0 times the design rule half pitch (see Figure 7). In both cases OPC has been applied to print all other features to size, which is the design rule half pitch for all wordlines and spaces, except SP0, for the select gates 3 times the half pitch and for the central space 6 times the half pitch.

Figure 7 also shows the aerial image contour of the flash wordline mask pattern that was measured with AIMSTM 45-193i on top of a CD-SEM image of the identical module. This picture exemplifies that the AIMSTM 45-193i is capable of accurately capturing the optical effects of a complex 2D-structure, closely matching the final image in resist.

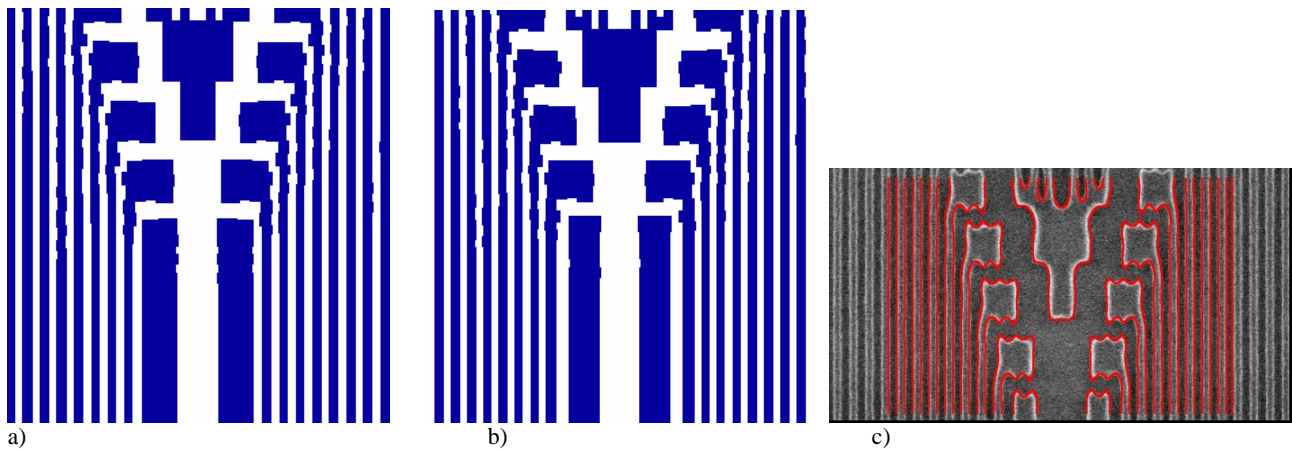


Figure 7 Different designs for SP0: a) 1.5 x minimum pitch, b) 2.0 x minimum pitch, c) Aerial image contour of SP0 1.5 design captured with AIMSTM 45-193i (red lines) on top of CD-SEM image. The landing pads and part of a dummy structure are also shown in these pictures

4.2. 40nm half pitch flash memory gate layer

The module on the mask with 40nm half pitch design rule (SP0 1.5 design) has been selected for detailed evaluation of the imaging performance as measured with AIMSTM on mask level and with CD-SEM on the wafer in resist. Figure 8 shows the measured CD in BF for both the attenuated and binary module in comparison to the designed CD. To

determine the aerial image CD's of the features in the gate layer first wordline 7 is evaluated. A threshold value is determined to print WL7 to size (i.e. 40nm). This threshold is used to calculate the CD's of the other features of interest. The feature sizes in the gate layer measured by CD-SEM and AIMSTM correspond well to each other. The maximum deviation is found to be 6nm, which is surprisingly small taking into account that no effort has been made to calibrate the metrology tools, the CD-SEM measurements are done in resist whereas the AIMS measurements are done in air, and that the measurements were not performed on exactly the same location in the flash structure (although very close to each other). The rms error has been calculated for the wordlines and spaces. The select gates are excluded, since they have a much higher targetCD. The rms error between SEM and AIMSTM measurements is 3.9nm for the attenuated module and 3.0nm for the binary module, which is significantly lower than the rms error between SEM measurements and the designed CD: 5.9nm (att) and 3.7nm (bin). This means that the AIMSTM 45-193i is a better predictor of the optical proximity effects observed on wafer level than the simulation model that was used here (Kirchhoff mask and LPM model), despite the fact that AIMSTM cannot capture any resist effects.

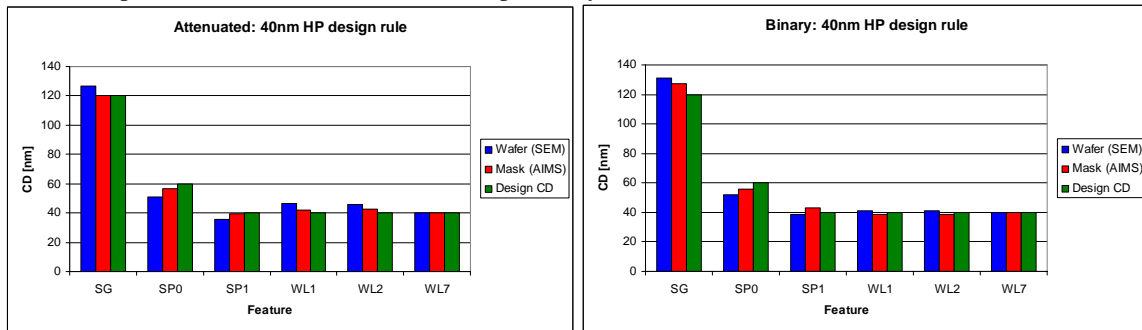


Figure 8 CD in BF for all evaluated features in the gate layer (40nm half pitch) as measured with CD-SEM on the wafer and with AIMSTM on mask level compared to the designed CD. The left picture shows the attenuated module, the right picture the binary module.

In Figure 9 the EL measured with CD-SEM and AIMSTM is compared for the attenuated and binary module. In both cases the AIMSTM measurements show a much larger EL than is observed on the wafer. This is as expected since the imaging characteristics of the photo resist, and the resist contrast in particular, play an important role in the final EL as measured on the wafer. The AIMSTM measurements also show some larger feature-to-feature variations in EL than measured in resist. If we zoom in further, we can see that the EL of WL1 and WL7 is clearly larger than the EL of SP1 and WL2 as measured with AIMSTM: 22.2% vs. 19.4% for the attenuated and binary measurements averaged. On wafer level this difference is reduced to 15.7% vs. 14.8%, but the trend picked up on mask level remains visible in resist. This can be explained by the fact that AIMSTM uses a threshold model (zero diffusion length) whereas the photo resist exhibits some image blur (effective acid diffusion length in the order of 15-25nm), which smoothens out these subtle variations in EL.

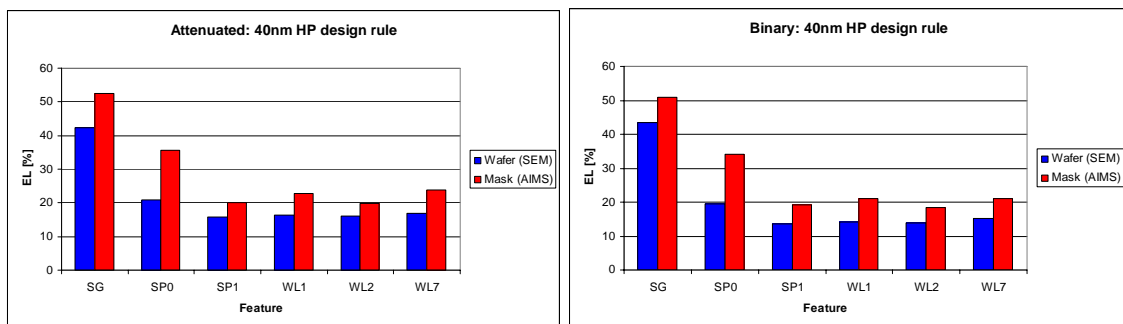


Figure 9 Exposure Latitude for all evaluated features in the gate layer (40nm half pitch) as measured with CD-SEM on the wafer and with AIMSTM on mask level. The left picture shows the attenuated module, the right picture the binary module. Note that the EL has been calculated based on the design value, i.e. 120nm for SG, 60nm for SP0 and 40nm for the other features.

Figure 10 shows the Bossung plots of all evaluated features in the 40nm flash gate layer for the attenuated and binary modules as measured with AIMSTM on mask level and in resist with CD-SEM. To convert the focus values as reported by AIMSTM 45-193i on mask level to focus values on wafer level we used an XT:1900Gi –specific mask-to-wafer

conversion factor, which deviates ~10% from the non-paraxial formula⁶ that is used in the AIMSTM software. The focus range over which the select gates show a good image integrity can be measured accurately by AIMSTM on mask level. Both the AIMSTM and CD-SEM measurements report a maximum depth-of-focus of 130nm for this focus-critical feature. The focus range of the other features is slightly overestimated by AIMSTM, since the aerial image measurements cannot capture resist effects like pattern collapse, which is one of the DoF-limiting factors on the wafer for the minimum resolution structures. However, the Bossung curvature of the aerial image Bossungs correspond well to the resist Bossungs, although the focus sensitivities are slightly underestimated.

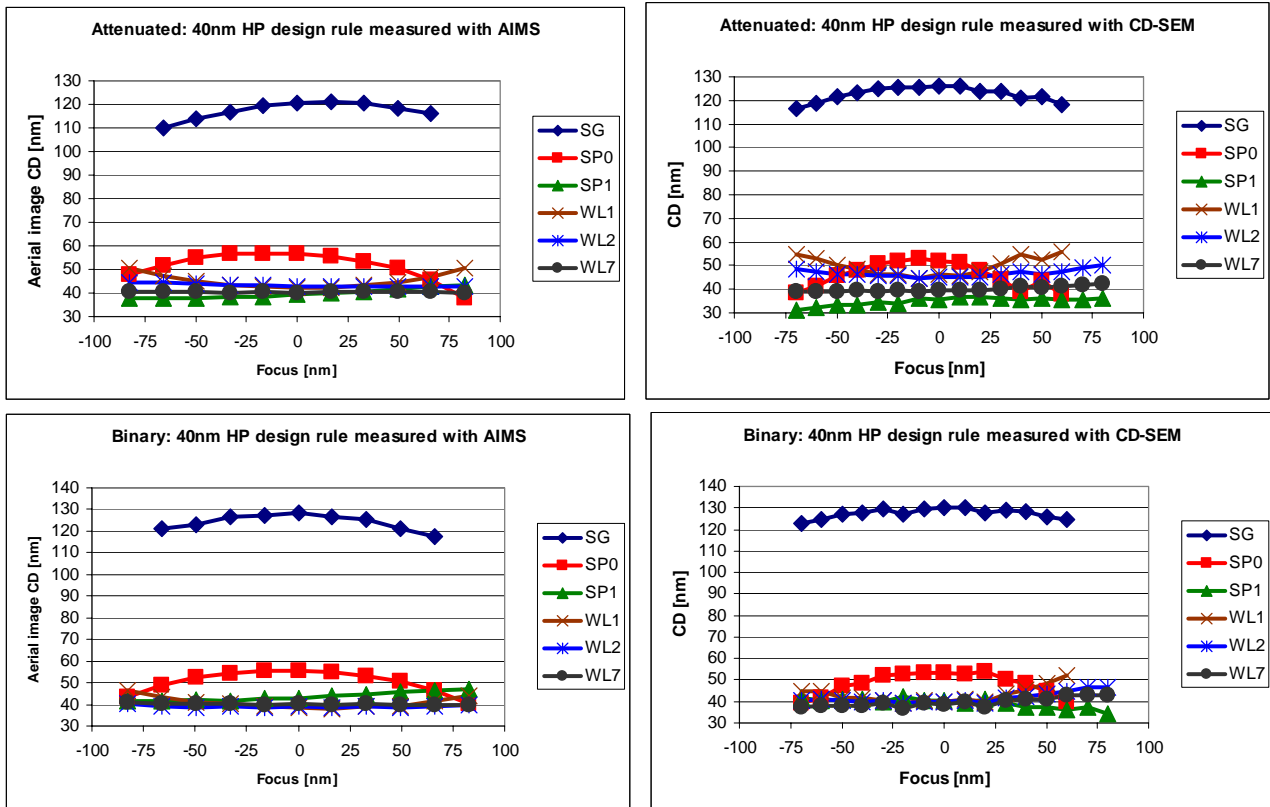


Figure 10 Bossung plots for all evaluated features in the gate layer for the 40nm half pitch flash modules. Top left: Att. module measured with AIMSTM on mask level (numbers are on 1x), Top right: Att. module measured with CD-SEM on the wafer, Bottom left: Bin. module measured with AIMSTM on mask level (numbers are on 1x), Bottom right: Bin. module measured with CD-SEM on the wafer.

Dusa et al. predicted that the imbalance in the near-field diffraction intensity in the vicinity of the select gates would lead to a feature-center shift through focus of the select gates and the adjacent 4 to 5 wordlines. This feature-center shift can be regarded as an intra-module overlay error coming from the design itself, in addition to intra-field and across wafer overlay errors coming from the scanner and the reticle. From the CD-SEM and AIMSTM measurements through focus the feature-center placement errors of the select gates, WL1 and WL2 have been determined. The center of the central space (denoted as SGSG in Figure 6) has been chosen as reference. A positive shift indicates that the line moves away from the center, i.e. in the positive x-direction for features on the right side of the central space and in the negative x-direction for features on the left side of the central space. Conversely, a negative shift indicates that the line moves towards the central space (see also Figure 11).

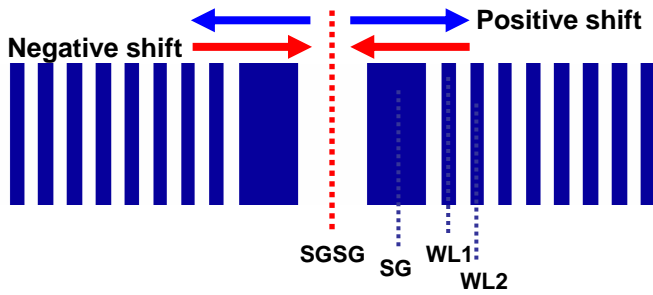
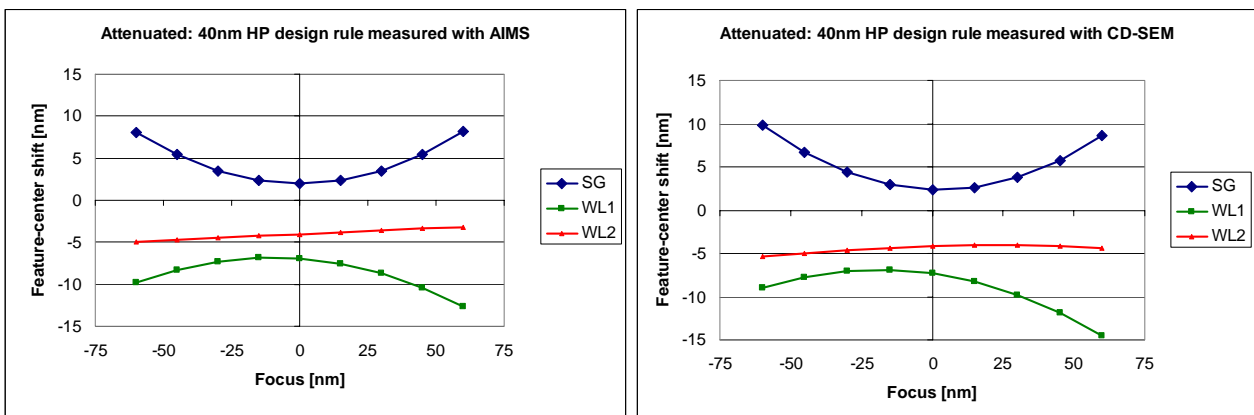


Figure 11 Definition of feature-center shift: A positive shift moves the line away from the center, a negative shift towards the center. The evaluated features are SG, WL1 and WL2.

Figure 12 shows the results for the attenuated and binary modules with 40nm half pitch design rule. The select gates have a positional shift of 2nm in best focus, which increases to ~9nm when going 60nm out of focus. Wordline 1 goes in the opposite direction of the select gates and shows a shift of -7nm in best focus and ~ -11nm when going 60nm out of focus. Wordline 2 shows the smallest shift, only -4nm in best focus, which remains almost stable through focus (~ -5nm when going 60nm out of focus).

If we assume that the overlay budget is 20% of the CD node (i.e. 8nm in this case), of which a 4nm error can be tolerated for these intra-module overlay errors, then it becomes clear that the positional shift consumes almost the total overlay budget, leaving no room for additional overlay errors from the scanner and the reticle. But also if it would be possible to compensate for the shift in best focus in the underlying active area, the focus range should be controlled within +/-45nm to stay within the 4nm placement error budget. This means that the required focus control is driven by the placement errors through focus rather than the CD variations. The differences between the binary and attenuated module are less than 0.5nm and are considered to be not significant.

Besides the lithographic implications that can be derived from Figure 12, a remarkable agreement between the AIMSTM measurements on mask level and wafer measurements with CD-SEM can be observed. The correlation plots in Figure 13 shows that the AIMSTM and CD-SEM data sets for both modules are statistically identical assuming a measurement error of 1.0nm 1 σ for CD-SEM and 0.4nm 1 σ for AIMSTM. These measurement errors include local CD variations due to wafer non-flatness and processing (CD-SEM), local mask CD variations (AIMSTM) and cumulative measurement errors from the calculation method of the placement error (adding line and space measurements). To arrive at these results we fitted the original measurement curves with a 2nd order polynomial fit to get rid of most of the measurement noise, centered best focus for 1:1 comparison and calibrated the central space (SGSG) size, which is the reference for the feature-center calculation.



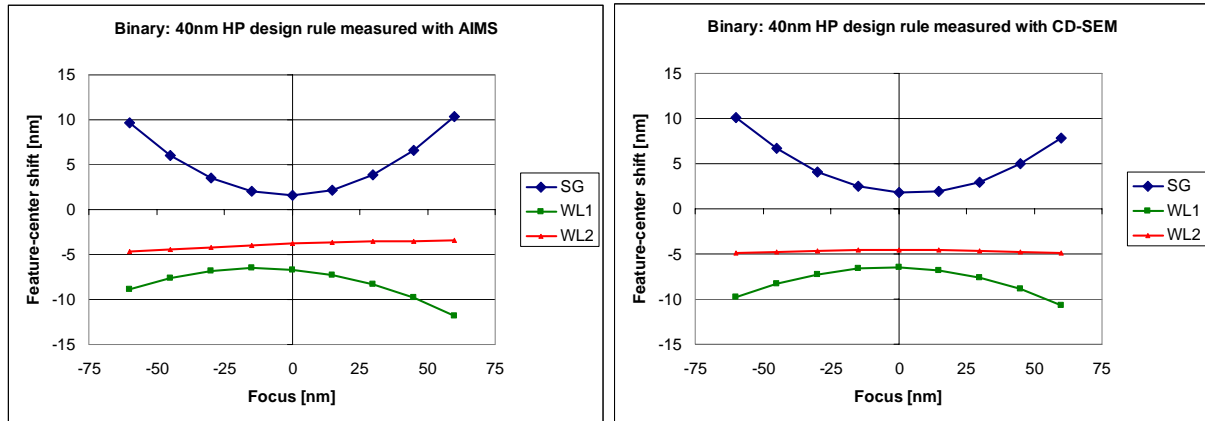


Figure 12 Feature-center placement error measured for SG, WL1 and WL2 for the 40nm half pitch flash modules. Top left: Att. module measured with AIMS™ on mask level (numbers are on 1x), Top right: Att. module measured with CD-SEM on the wafer, Bottom left: Bin. module measured with AIMS™ on mask level (numbers are on 1x), Bottom right: Bin. module measured with CD-SEM on the wafer.

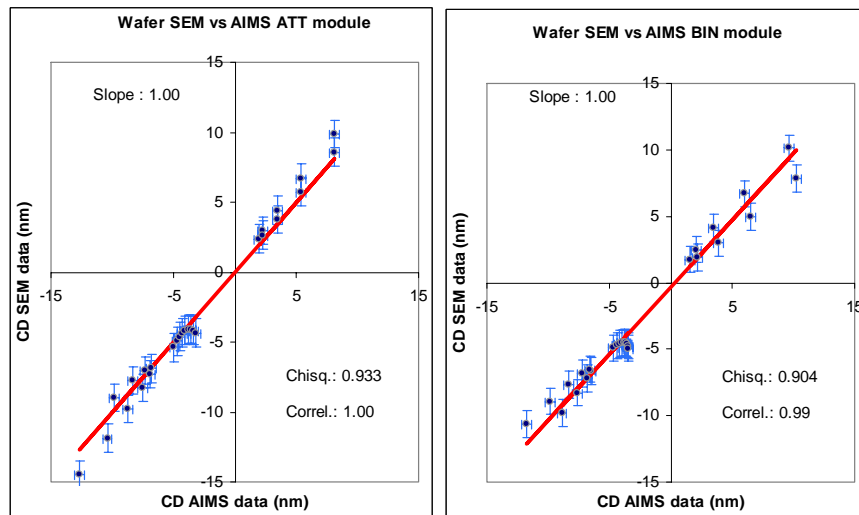


Figure 13 Correlation plots of measured feature-center placement errors between wafer (CD-SEM) and mask (AIMS™) for the 40nm half pitch flash modules. Left: Attenuated module, Right: Binary module.

4.3. De-sensitizing the Flash wordline mask pattern

One of the possibilities to de-sensitize the flash wordline mask pattern for feature-center placement errors is by varying the space between the select gates and the first wordline. Two designs with 1.5 and 2.0 times the design rule half pitch for SP0 have been studied in resist for the 39 and 40nm modules.

Figure 14 shows the feature-center shift of SG, WL1 and WL2 for both designs of the attenuated and binary 39nm modules. Again we fitted the original measurement curves with a 2nd order polynomial fit to get rid of most of the measurement noise. An increase of SP0 results in a reduction of the feature-center shift for wordline 1, but the placement error of wordline 2 and the select gates increases slightly. However, for the attenuated module the focus sensitivity of the SG shift reduces as well. So if the shift in BF can be correctly compensated, this design would give the largest usable focus range, assuming a 10% (3.9nm) intra module overlay budget: 110nm focus range for the 2.0 design vs. 90nm focus range for the 1.5 design. This does not hold for the binary module, which shows approximately the same focus sensitivities for SG, WL1 and WL2. So for both binary SP0 – designs the allowable focus range is 90nm.

In Figure 15 the results for the 40nm modules are shown. The effects observed for the 39nm modules are more pronounced: The increase of space SP0 results in a significant reduction of the feature-center shift for wordline 1, while the placement error of WL2 and SG increases. In the attenuated case the focus sensitivity of the SG shift is almost completely removed. The focus sensitivity of the WL1 shift is reduced as well, while it remains the same for WL2. With the correct compensation scheme this results in a usable focus range of 140nm for the 2.0 design, vs. 90nm focus range for the 1.5 design. For the binary module the focus sensitivities are slightly reduced by increasing SP0, however this does not result in a larger focus tolerance: 90nm focus range for both designs.

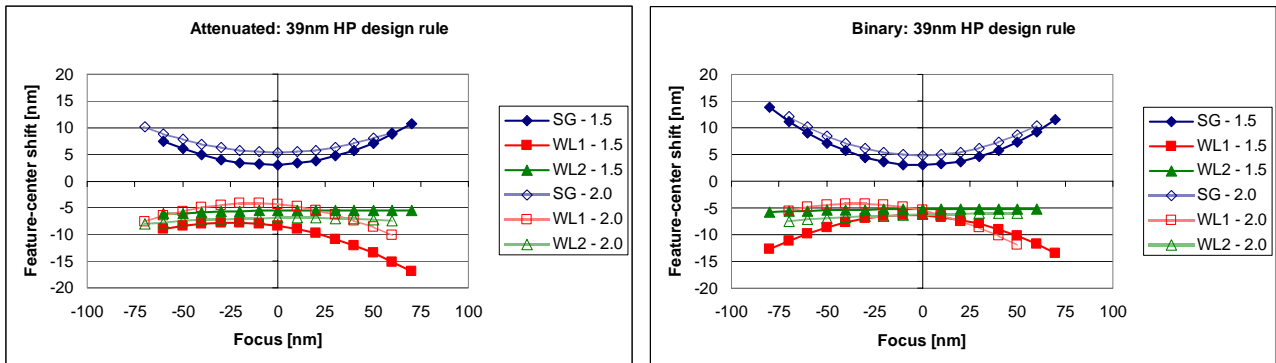


Figure 14 Feature-center placement error of SG, WL1 and WL2 measured on the wafer with CD-SEM for 39nm half pitch design rule with space $SP0 = 1.5 \times 39\text{nm}$ and $2.0 \times 39\text{nm}$. Left: Attenuated module, Right: Binary module

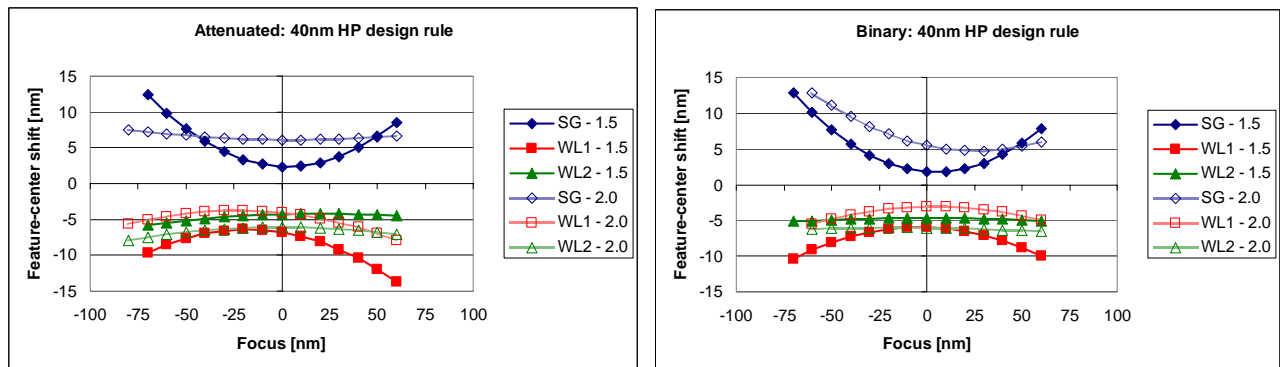


Figure 15 Feature-center placement error of SG, WL1 and WL2 measured on the wafer with CD-SEM for 40nm half pitch design rule with space $SP0 = 1.5 \times 40\text{nm}$ and $2.0 \times 40\text{nm}$. Left: Attenuated module, Right: Binary module

Changing space $SP0$ does not only impact the feature-center shift, but also influences depth of focus and exposure latitude. Figure 16 shows the EL for the attenuated and binary 39 and 40nm modules. Increasing $SP0$ results in an improvement of the EL for all dose-critical features in the gate layer of the attenuated module. This can be attributed to the change in OPC needed to print all features to size. The improvement is not observed for the binary module, which is as expected since the EL of binary features is less sensitive for line biasing, as also observed in a previous study⁷. The large increase of the EL of $SP0$ itself is misleading since the EL was calculated based on the design CD, which is 80nm for the 2.0 design and 60nm for the 1.5 design. In fact, the dose sensitivity is the same for both 40nm designs: 3.7nm/mJ for the attenuated modules and 4.0nm/mJ for the binary modules. For $SP0$ in the 39nm modules the dose sensitivity is slightly lower for the 2.0 design.

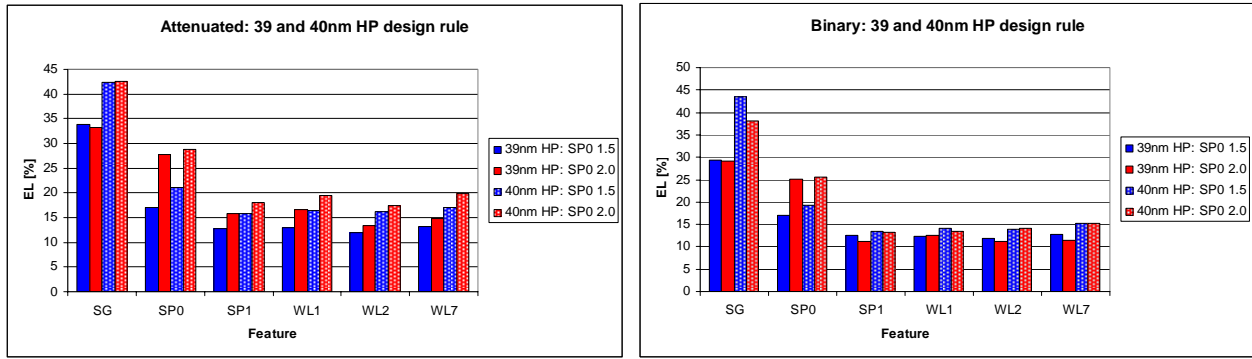


Figure 16 Exposure Latitude for all evaluated features in the gate layer (40nm half pitch) with space $SP0 = 1.5 \times 40\text{nm}$ and $2.0 \times 40\text{nm}$ as measured with CD-SEM on the wafer. Left: Attenuated module, Right: Binary module

Figure 17 shows the Bossung plots for the attenuated and binary 40nm modules with 1.5 and 2.0 $SP0$ design. The increase of $SP0$ affects especially the Bossung curvature of $SP0$ itself by removing the focus sensitivity almost completely ($SP0$ prints close to isofocal) for both the attenuated and binary modules. But also the focus sensitivity of $WL1$ is significantly reduced. From the Bossung plots it is also visible that the OPC worked out better for the binary modules than for the attenuated modules, and also better for the $SP0$ 2.0 design than for the $SP0$ 1.5 design. The 39nm half pitch attenuated and binary modules with 1.5 and 2.0 $SP0$ design show the same trends as observed in the 40nm half pitch data when it comes to the Bossung curvature (the 39nm Bossungs are not included due to space restrictions). This indicates that the optimization strategy is valid for multiple pitches.

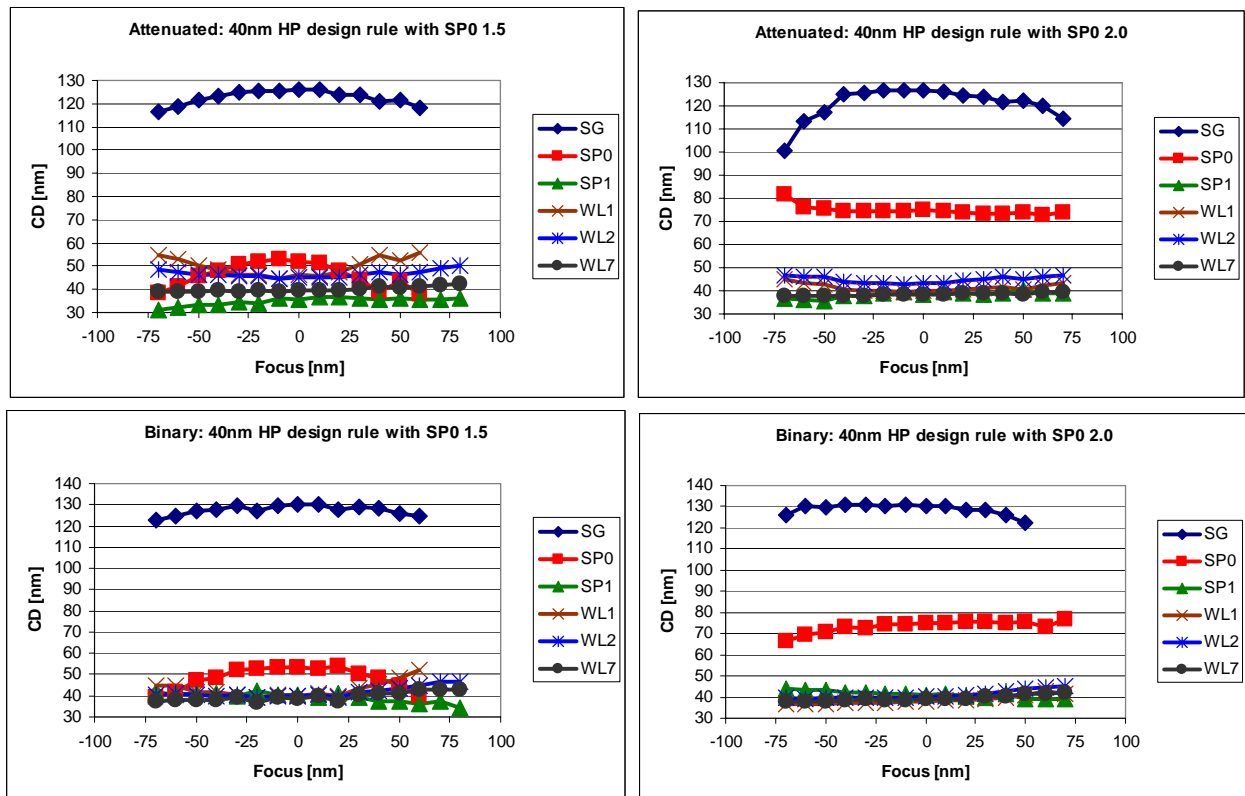


Figure 17 Bossung plots for all evaluated features in the gate layer (40nm half pitch) with space $SP0 = 1.5 \times 40\text{nm}$ and $2.0 \times 40\text{nm}$ as measured with CD-SEM on the wafer. Top left: Attenuated 1.5 module, Top right: Attenuated 2.0 module, Bottom left: Binary 1.5 module, Bottom right: Binary 2.0 module.

5. Conclusions

The AIMS™ 45-193i aerial image measurement system has been demonstrated to be a valuable tool to characterize the imaging performance of Flash memory masks. Important lithographic parameters such as MEEF, OPE, EL, DOF and placement errors can already be quantified on mask level before the mask is actually exposed on a scanner. By comparing AIMS™ measurements to wafer prints using an XT:1900Gi scanner it has been experimentally proven that feature-center placement errors in Flash memory designs are optical induced effects, which are inherent to the feature design. It has been shown that AIMS™ measurements can accurately capture these optically induced mask effects and therefore help to distinguish between mask effects and scanner or resist effects in lithography. The final imaging performance on the wafer is also heavily dependent on the photo resist stack used, which is naturally not taken into account in AIMS™ measurements. However, the AIMS™ measurements of MEEF, OPE, EL and DOF predict the correct trends and can be used as indicative. Feature-center placement errors induced by the design on the mask can be accurately measured by AIMS™ and mapped almost perfectly on wafer measurements with CD-SEM. DoF-limiting factors such as image reversal can also be measured accurately.

Feature-center placement errors have been shown to be inherent to the design of the flash wordline mask pattern, consuming a large part of the overlay budget. To prevent impact on the final device performance this effect should be taken into account in the design of flash memory layout.

We also showed that the flash wordline mask pattern can be de-sensitized for placement errors by increasing the space between the select gates and wordline 1. This also results in a larger EL of the dose-critical features for the attenuated modules and a reduced Bossung curvature of SP0 and WL1 for both the attenuated and binary modules.

Good image integrity over 130nm focus range has been demonstrated for 39 and 40nm half pitch design rule flash memory gate structures exposed with an XT:1900Gi hyper-NA immersion system. This shows the viability of the XT:1900Gi to support the demands of the Flash memory market for 40nm half pitch and possibly below⁸ for high volume manufacturing.

6. Acknowledgements

The authors would like to thank Carl Zeiss SMS for making this correlation work possible, Brid Connolly from AMTC-Toppan for the support, technical suggestions and the effort to get the test mask delivered on very short notice. We furthermore would like to acknowledge the '1900 apps team' for carrying out the exposures on the XT:1900Gi, a special thanks to Mariette Berende-Hoogendijk and other members of the CD-SEM metrology group for the CD-SEM measurements and pictures.

REFERENCES

-
- ¹ A. Erdmann et al, "Rigorous electromagnetic field mask modeling and related lithographic effects in the low k1 and ultrahigh numerical aperture regime", J. Micro/Nanolith., MEMS MOEMS 6, 031002 (2007)
 - ² M. Dusa et al, "An integrated lithography concept with application on 45nm ½ pitch flash memory devices", Optical Microlithography XIX, Proceedings of SPIE, Vol. 6154 (2006)
 - ³ A. Zibold et al, "First results for hyper NA scanner emulation from AIMS™ 45-193i", Proceedings of SPIE, Vol. 6283, 628312 (2006)
 - ⁴ P. De Bisschop et al, "Using the AIMS 45-193i for hyper-NA imaging applications", Proceedings of SPIE, Vol. 6730, 67301G (2007)
 - ⁵ J. van Schoot et al, "The mask error factor: causes and implications for process latitude", Optical Microlithography XII, Proceedings of SPIE, Vol. 3679 (1999)
 - ⁶ C. A. Mack et al, "Exploring the capabilities of immersion lithography through simulation", Proceedings of SPIE, Vol. 5377, 428 (2004)
 - ⁷ E. van Setten et al, "Masks for Flash Memory Gates for the 45nm node: Binary or attenuated?", Proceedings of SPIE, Vol. 6533, 65330L (2007)
 - ⁸ E. van Setten et al, "The Flash memory battle: How low can we go?", to be published in Proceedings of SPIE, 2008