

EUV mask stack optimization for enhanced imaging performance

Eelco van Setten^a, Dorothe Oorschot^a, Cheuk-Wah Man^a, Mircea Dusa^b, Robert de Kruijff^a, Natalia Davydova^a, Kees Feenstra^a, Christian Wagner^a,
Petra Spies^c, Tristan Bret^c, Markus Waiblinger^c

^aASML Netherlands B.V., De Run 6501, 5504 DR Veldhoven, The Netherlands

^bASML Belgium bvba., Kapeldreef 75, 3001 Leuven, Belgium

^cCarl Zeiss SMS GmbH, 07740 Jena / 64380 Roßdorf, Germany

EUVL requires the use of reflective optics including a reflective mask. The reticle blank contains a reflecting multilayer, tuned for 13.5nm, and an absorber which defines the dark areas. The EUV mask is a complex optical element with many more parameters than the CD uniformity of the patterned features that impact the final wafer CDU. Peak reflectivity, centroid wavelength and absorber stack height variations need to be tightly controlled for optimum performance. Furthermore the oblique incidence of light in combination with the small wavelength compared to the mask topography causes a number of effects which are unique to EUV, such as an H-V CD offset and an orientation dependent pattern placement error. These so-called shadowing effects can be corrected by means of OPC, but also need to be considered in the mask stack design.

In this paper we will show that it is possible to improve the imaging performance significantly by reducing the sensitivity to mask making variations such as capping layer thickness and absorber stack height variations. The impact of absorber stack height variations on CD and proximity effects will be determined experimentally by changing the local absorber stack height using the novel e-beam based reticle repair tool MeRiT[®] HR 32 from Carl Zeiss in combination with exposures on ASML's alpha demo tool. The impact of absorber reflectivity will be shown experimentally and used to derive requirements for the reticle border around the image field, as well as possible correction techniques.

Key words: EUV lithography, imaging, masks

1. Introduction

EUVL requires the use of reflective optics including a reflective mask. The reticle consists of a substrate with ultra low expansion coefficient (ULE), a reflective multilayer that is tuned for 13.5nm wavelength, and an absorber which defines the dark areas. An EUV mask is a complex optical element with many more parameters than the CD uniformity of the patterned features that impact the final wafer CDU. The multilayer (ML) stack, which typically consists of 40-50 layers of Mo-Si, needs to be tightly controlled for peak reflectivity and centroid wavelength variations. The absorber stack needs to have a uniform and precisely determined height across the wafer to minimize CD errors while taking the flare level from EUV reflection from the absorber into account. Furthermore, the oblique incidence of light in combination with the small wavelength compared to the mask topography causes a number of effects which are unique to EUV, such as an H-V CD offset and an orientation dependent pattern placement error. These so-called shadowing effects can be corrected by means of OPC, but also need to be considered in the mask stack design. The imaging performance of the mask can be optimized by an integral approach, taking the whole mask stack (ML, capping and absorber stack) into account.

In this paper will look into the impact of absorber height variations on 27nm dense L/S in resist by means of wafer prints on the Alpha Demo Tool. Rigorous simulations are performed for comparison to the experimental data and to evaluate the possibilities for mask stack optimization for the NXE:3100. Furthermore, we will look at the impact of EUV absorber reflectivity on CD uniformity as function of die-spacing and possible correction methods.

2. Absorber height variation

From rigorous simulations it is known that variations in the absorber stack height at reticle level result in CD changes in resist at wafer level^{1,2}. The wafer CD decreases with decreasing absorber thickness while oscillating with a period equal to $\sim\lambda/2$ (λ is the exposure wavelength).

The impact of absorber height variations at reticle level on the CD at wafer level has been investigated experimentally by means of a dedicated test reticle. The reticle has a designed absorber height of 44nm low-reflective TaBN and contains 27nm dense L/S grating (at 1x). It was treated with the Zeiss MeRiT HR 32 reticle repair tool³, thinning the absorber of 10 line sections of 2 μ m inside the L/S grating with \sim 2nm steps by means of a focused electron beam.

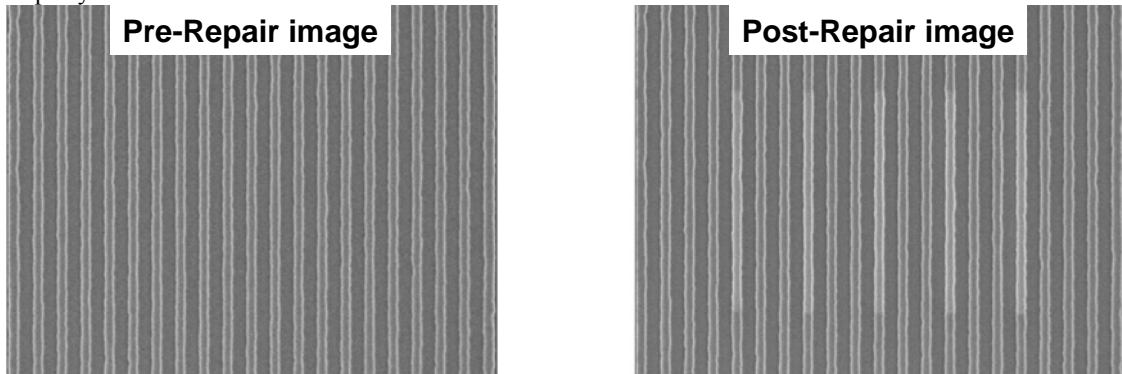


Figure 1 shows the SEM images of the 27nm dense L/S grating on the reticle before and after repair. Both gratings with horizontal and vertical lines are treated at (almost) the same location on the mask, using the MeRiT pattern copy repair function. The lines after repair are measured with AFM to determine accurately the amount of absorber that has been etched away. The measurement results for the vertical lines are shown in Figure 2 below.

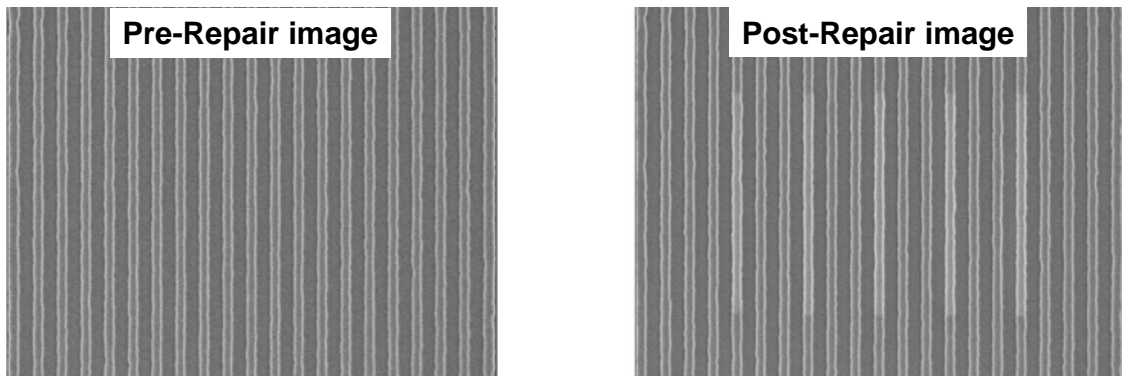


Figure 1 SEM images of the 27nm dense L/S gratings on the reticle before and after repair. The repaired lines show up as bright sections of the line, which are 2 μ m long and 648nm apart (every 3rd line). The grating contains two sections with 5 treated lines, resulting in 10 line parts with a different absorber height in steps of \sim 2nm.

AFM results

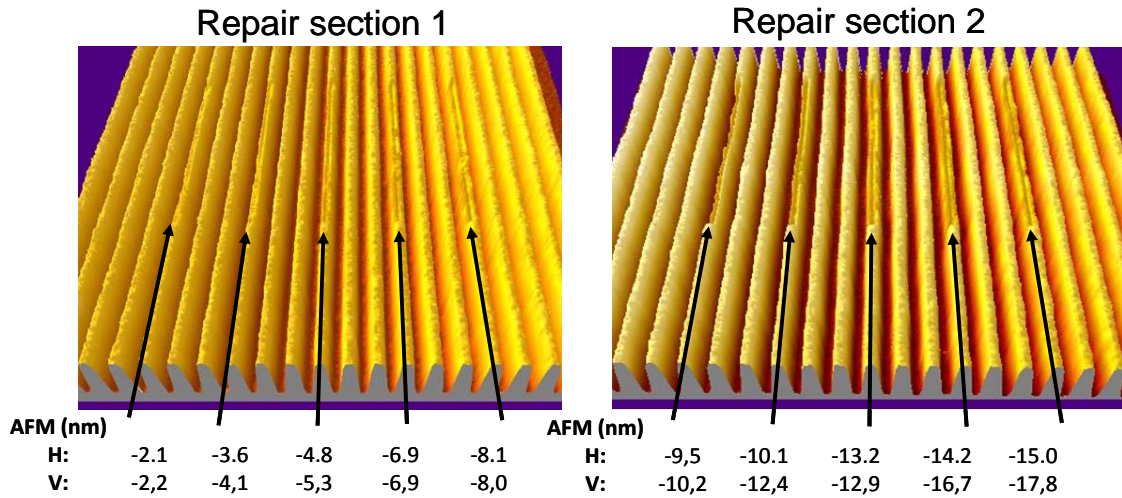


Figure 2 AFM measurement results of the repaired line sections. Per treated line the difference with respect to the nominal line height is shown, ranging from -2.1 to -15.0nm for three horizontal L/S grating and from -2.2 to -17.8nm for the vertical L/S grating. The AFM pictures show the vertical L/S grating.

After repair the reticle was exposed on the Alpha Demo Tool (ADT) in the IMEC cleanroom facility in Leuven, Belgium. The ADT is a full field step-and-scan exposure system⁴ with an NA of 0.25 for extreme ultraviolet lithography (EUVL) and is being used for EUVL process development and integration. A Focus-Exposure-Matrix with a nominal dose of 8.5mJ/cm² was exposed on bare Si wafers coated with 50nm Shin Etsu SEVR-140 resist. The CD measurements on the wafer were done with the Hitachi CG 4000. The SEM was programmed to measure the line parts that correspond to the etched lines on the reticle through focus and dose. In addition, an untreated part of the 5 lines was measured for reference.

The SEM images of the L/S gratings in resist show a high line width roughness which makes an accurate analysis of the line width as function of absorber height difficult, as can be seen from Figure 3. This image shows a part of the wafer where the treated lines on the mask do not print anymore, while the rest of the line still prints to target to illustrate the impact of a reduced absorber height on the wafer CD.

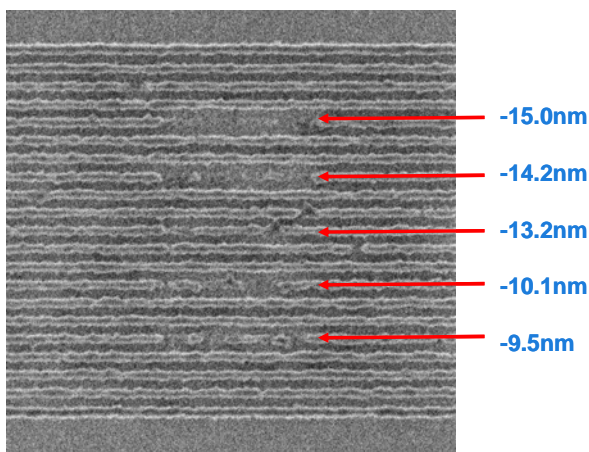


Figure 3 SEM image of wafer print of treated lines on the mask. The line parts with lowest absorber height disappear while the untreated lines still print to target.

To reduce the noise in the data the CD measurements have been averaged through focus, resulting in CD versus etch time (absorber height) curves for multiple dose values. Then the CD change relative to the reference absorber height (of 44nm) has been calculated per dose value and averaged through dose, as illustrated in Figure 4 below.

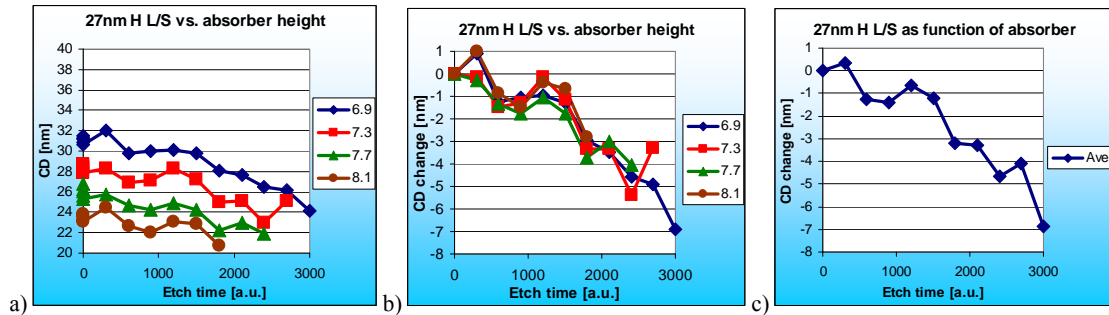


Figure 4 a) To reduce the noise level the CD SEM data is first averaged through focus and plotted as CD vs. etch time per dose step, b) then the relative CD change w.r.t. the nominal value per dose step is calculated. c) Finally the relative CD data is averaged through dose to arrive at the CD as function of etch time / absorber height.

Rigorous simulations (Prolith X3.1) using a calibrated resist model were performed for comparison to the experimental data. The absorber stack consists of 30nm TaBN and 14nm TaBO on a 2.5nm Ru capping layer. We used n&k values from the cxro-website⁵ (see Table 1). In the simulation first the TaBO DUV ARC was ‘etched’ away and then the TaBN absorber was thinned to 25nm, corresponding to the lowest absorber height on the mask after repair. Figure 5 shows the simulated CD response as function of the absorber height. The curves show a clear swing behavior, with the period equal to $\sim\lambda/2$. Furthermore, a general decrease in wafer CD with absorber height can be observed, which is more pronounced for the horizontal features than the vertical features. It should be noted that the simulations assumed a 1.2nm HV bias (1x), which was not sufficient to print H and V to target at 44nm absorber thickness.

Table 1 Absorber, capping layer thickness and n&k- values assumed in the rigorous simulations.

Material		n-value	k-value	thickness (nm)
DUV ARC	Ta8BO	0.9390	0.0418	14
Absorber	Ta8BN	0.9392	0.0412	30
Capping	Ru	0.8863	0.0171	2.5

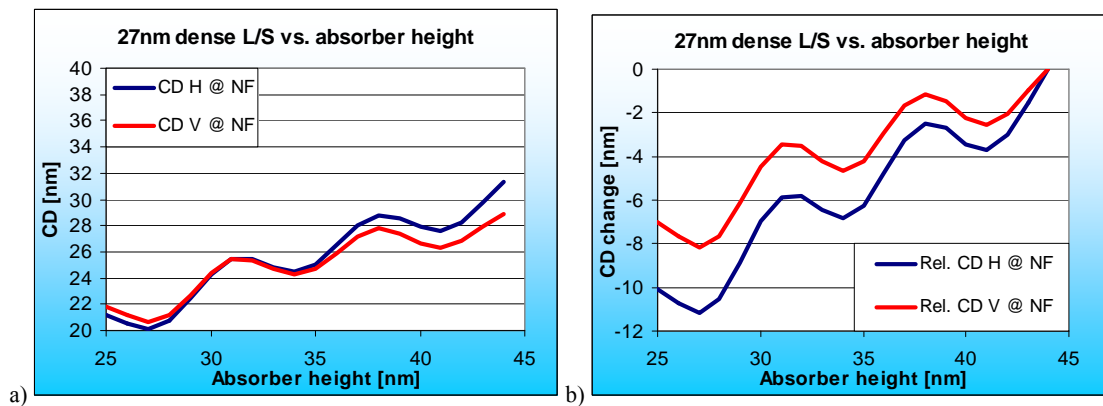


Figure 5 a) Simulated CD for 27nm dense L/S as function of absorber height, b) CD change w.r.t. reference (44nm absorber) as function of absorber height

The simulated CD as function of absorber height is compared to the experimental data in Figure 6 below. To arrive at these results the nominal absorber height was changed to 45nm (i.s.o. 44nm), which is within the tolerance of the absorber coating process, and the reference CD of the H-lines was allowed to float (whole curve was shifted downwards with 2 nm to compensate for a measured HV offset on wafer level that could not be explained from the available mask CD data). After these modifications the experimental data matches well with the simulated curves within the measurement accuracy over almost the entire absorber height range. From this we conclude that the swing behavior observed in the simulations is real and should be considered for mask stack specifications. The simulated slope of the curves is ~ 0.4 (V) – 0.5 (H) nm CD

change per nm absorber height change, while the local slope varies between -0.75 and 1.8nm/nm . This means that, depending on the location in the swing curve, small absorber height variations can result in significant CD errors on the wafer, comparable to CD errors from line width variations on the mask. This also means that line height roughness after patterning the mask will contribute to LWR on the wafer with a similar transfer function⁶ as regular line width roughness at reticle level. A thorough evaluation of the magnitude of this effect is outside the scope of this work, but should be considered in a mask LWR budget. Both the wafer CD variation and LWR due to absorber height variations can be minimized by choosing the correct nominal absorber height, e.g. in a minimum of the CD swing curve.

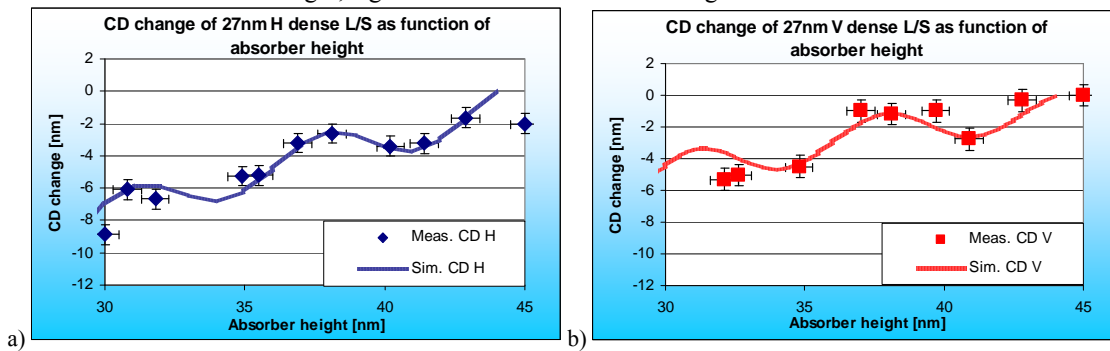


Figure 6 Comparison between simulations and experimental data of the CD change as function of absorber height for 27nm L/S. a) Horizontal L/S, b) Vertical L/S

3. Mask stack optimization

To explore the possibilities of choosing an optimized absorber height further, rigorous simulations have been performed on 27p54nm and 27p189nm H & V L/S features using $NA=0.25$, $\sigma = 0.8$ conv, as well as 24p48nm, 24p168nm, 48p144nm H&V L/S features using $NA=0.25$, $\sigma = 0.2/0.8$ Dipole-75-X/Y. The 48p144nm horizontal L/S are printed with a dipole-X setting and vice versa for the vertical L/S to evaluate the impact on features with a relaxed dimension orthogonal to the critical features in the design (e.g. wordlines vs. periphery). The simulations were done using a calibrated full resist model for Shin Etsu SEVR-40 in combination with a 5-pass simulation, taking 5 discrete wavelengths with different weighting into account (see Figure 7). The absorber thickness was varied between 51 and 61nm, the capping layer thickness between 2.0 and 3.0nm.

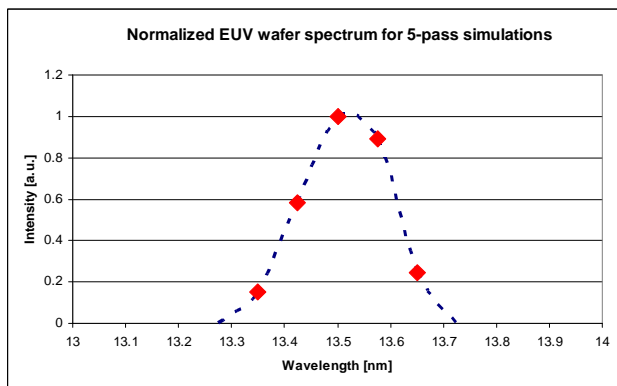


Figure 7 Normalized EUV source spectrum at waferlevel. The red dots represent the 5 discrete wavelengths that are used for full resist simulations.

The CD response for absorber thickness variations on a 40 ML model stack is shown in Figure 8 for both the 27nm L/S with conventional illumination and the 24nm L/S with Dipole illumination. The CD response shows a swing curve with an amplitude of more than 3nm for the 27nm horizontal dense L/S and $\sim 2\text{nm}$ for the 24nm dense L/S. The iso lines are less sensitive to absorber thickness variations and have a swing amplitude of $\sim 1.5\text{nm}$. The position of the swing minima and maxima are found to be the same for all

features. An absorber thickness of 55nm corresponds to a minimum in EUV absorber reflectivity and gives the lowest overall CD variation for +/-1nm absorber height variation (< ~0.7nm in all cases).

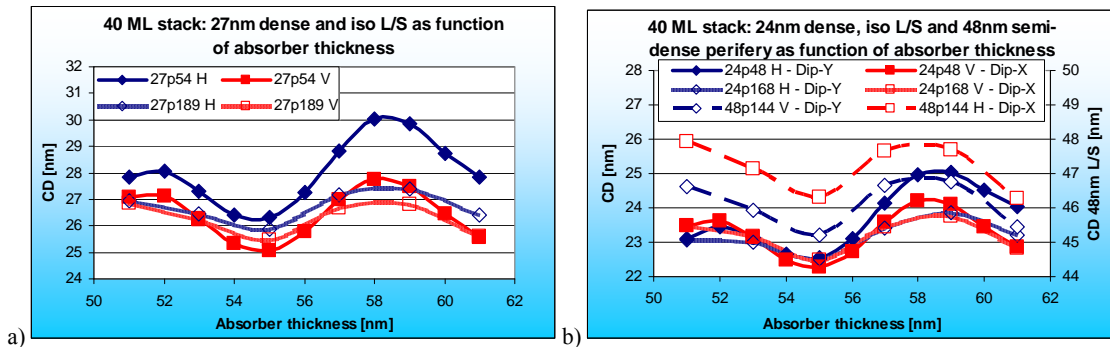


Figure 8 CD as function of absorber thickness for 27p54, 27p89nm H&V L/S with conventional ($\sigma=0.8$) illumination and for 24p48, 24p168, 48p144nm H&V L/S with Dipole-75-X/Y ($\sigma=0.2/0.8$) illumination. The mask ctw50 is 13.53nm, the capping layer thickness is 2.5nm. a) 40 ML model stack – 27nm L/S, b) 40 ML model stack – 24nm L/S with Dipole

Figure 9 shows the dense-iso bias as function of absorber thickness for the 27nm, 24 and 48nm L/S features. The simulated dense-iso bias change for 27nm horizontal L/S is up to 2nm going from 55 to 59nm absorber thickness. Thus the absorber thickness needs to be tightly controlled as well across the mask and from mask-to-mask to prevent proximity matching errors. Furthermore, the absorber thickness needs to be considered for OPC determination.

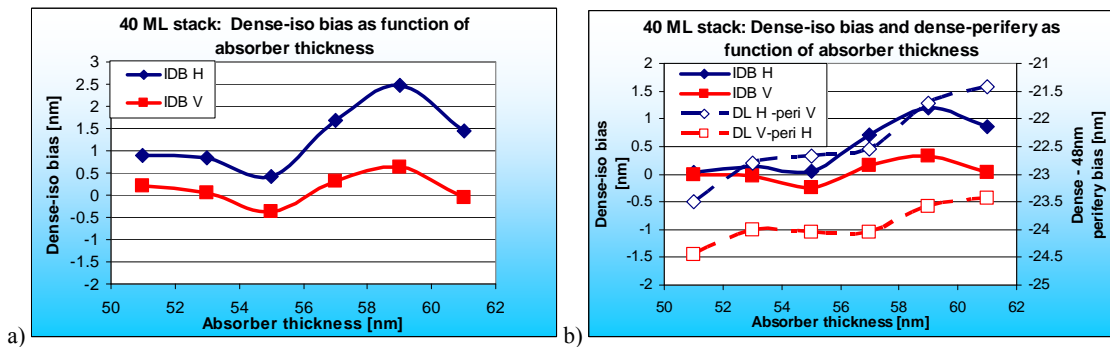


Figure 9 Dense-iso bias as function of absorber thickness for 27p54, 27p89nm H&V L/S with conventional ($\sigma=0.8$) illumination and for 24p48, 24p168, 48p144nm H&V L/S with Dipole-75-X/Y ($\sigma=0.2/0.8$) illumination. The mask ctw50 is 13.53nm, the capping layer thickness is 2.5nm. a) 40 ML model stack – 27nm L/S, b) 40 ML model stack – 24nm L/S with Dipole

The absorber thickness variations on a state-of-the-art mask was measured after patterning on designated pads using a FEI SNP-XT Stylus Nanoprofilometer with a measurement repeatability of 0.4nm 3σ and +/-1nm absolute accuracy, calibrated against NIST standards. The mean value was found to be 55.4nm with a range of 0.5nm across the entire image field of the mask, see Figure 10. Combined with the CD and dense-iso bias simulations, this would result in an expected CD impact on wafer level of < 0.5nm (27nm L/S) / < 0.3nm (24nm L/S) and dense-iso bias of < 0.3nm (27nm L/S) / < 0.15nm (24nm L/S). This is sufficient to support 27 and 24nm node imaging.

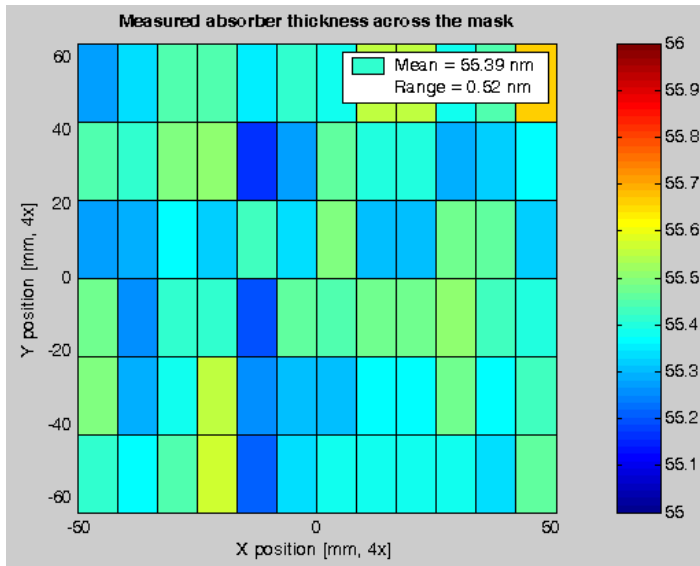


Figure 10 Measured absorber thickness across the mask after patterning.

The impact of absorber height variations on OPC was tested experimentally by exposing two identical masks with a slightly different absorber height on the Alpha Demo Tool at IMEC. Mask A has a measured absorber height of 55.4nm, mask B 58nm. Process windows were measured for 27nm dense and iso L/S. Figure 11 shows the measured best energy for both masks after correction for the measured CD difference at mask level. Mask A is found to have an 8% lower dose-to-size than mask B, while the best energy (BE) is the same for the iso lines. If we plot the dense-iso bias at a fixed dose of 12mJ/cm² for both masks, then we see a difference of ~1.5nm between the 2 absorber heights (Figure 12). The measured value matches well with the expected value based on rigorous simulations.

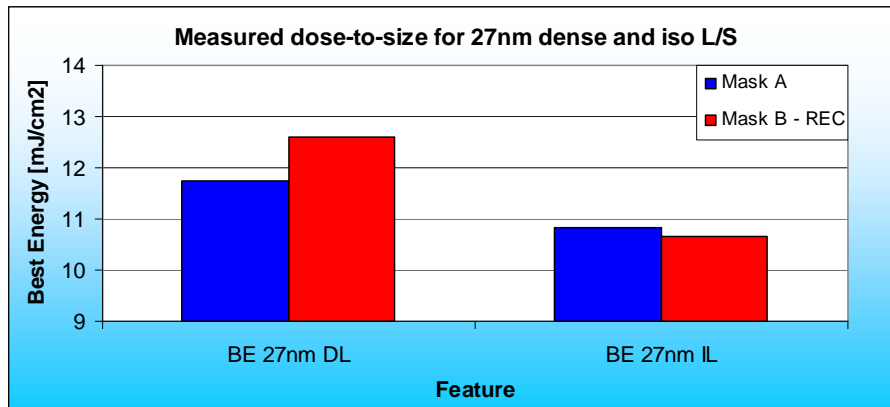


Figure 11 Dose-to-size for 27nm dense and iso L/S for identical masks with a different absorber height, exposed on the same tool.

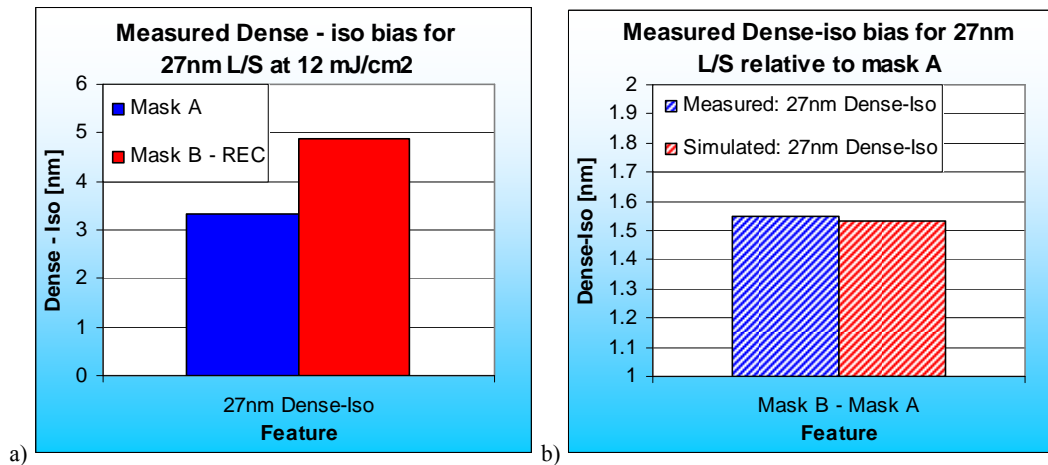


Figure 12 a) Measured Dense-iso bias for 27nm L/S for mask A and B b) Measured Dense-iso bias for 27nm L/S compared to simulations for mask A and B

In Figure 13 the CD response for capping layer variations is shown. The CD sensitivity is found to be low in general, but interacts with the absorber height. The CD variation due to +/-0.2nm capping layer variation is between ~1.0nm for the horizontal L/S with 57nm absorber height and ~3nm capping layer thickness, while it reduces to <0.1nm for 55nm absorber and 2.4nm capping layer. This means it is possible to tune the absorber and capping layer for minimum CD sensitivity, and hence a better imaging performance or larger tolerances towards mask making errors. The whole mask stack, including multilayer, should be taken into account for the optimum result⁷.

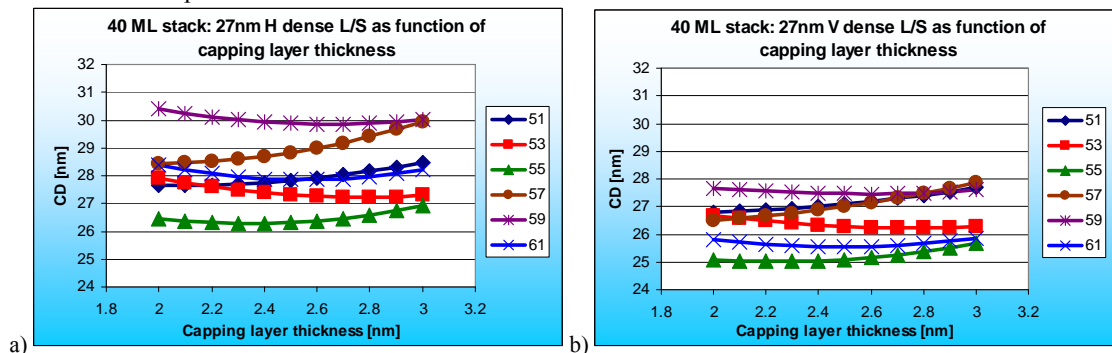


Figure 13 CD as function of capping layer thickness for 27nm H&V dense L/S with conventional ($\sigma=0.8$) illumination for several absorber heights. The mask ctw50 is 13.53nm. a) Horizontal L/S, b) Vertical L/S

4. Absorber EUV reflectivity requirements

When optimizing the mask stack for imaging, also the EUV reflectivity of the absorber should be taken into account. A high EUV absorber reflectivity can result in large CD errors in the reticle black border area where adjacent fields meet^{8,9}. Figure 14 shows that the EUV flare from the absorber leakage is dependent on the absorber thickness and shows a swing behavior with local reflectivity minima and maxima. We performed an experiment on the Alpha Demo Tool at IMEC using the same test reticle as for the reticle repair experiment described above. The nominal absorber thickness of 44-45nm is expected to reflect between 2.8 and 2.1% of the incoming EUV light. Taking the expected EUV broad band spectrum at waferlevel into account this translates to an EUV flare level of 4.7-3.6% coming from the absorber, using the n&k values from Table 1. The impact of the absorber reflectivity in the reticle black border area on imaging was tested on 32nm dense L/S using Shin Etsu SEVR-59 resist with a 65nm resist thickness on bare Si wafers. A full slit of 26mm was exposed with spacing between the dies that was varied between 0 and 3000 μ m with increasing step size (see Figure 15).

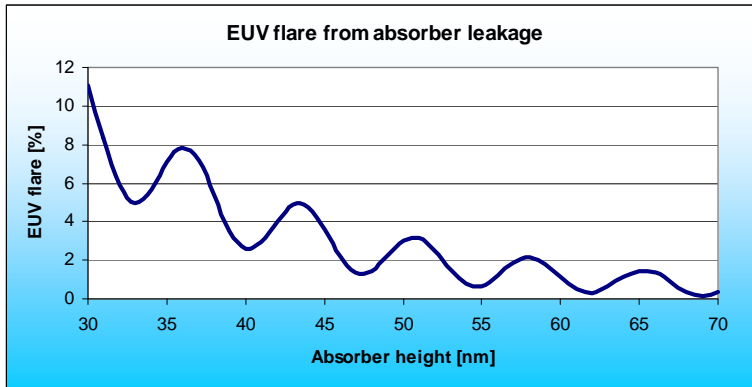


Figure 14 Simulated EUV flare from the absorber leakage as function of absorber height.

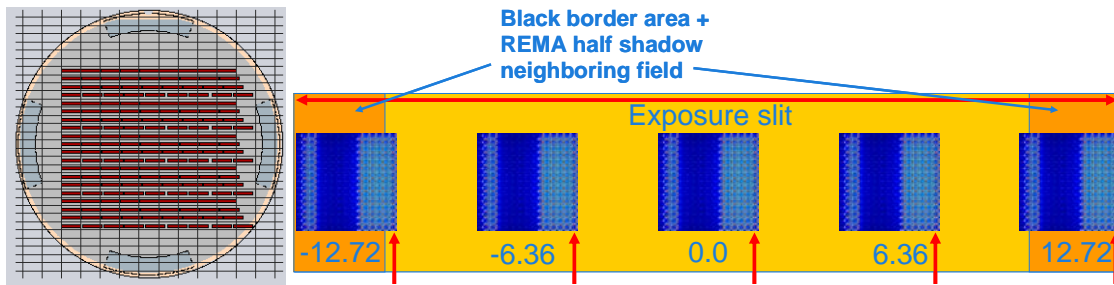


Figure 15 Wafer layout of die-spacing experiment. The spacing between the fields is varied from 0 to 3000 μm with increasing step size. There are 5 identical blocks for averaging. All fields are exposed at dose-to-size and best focus for 32nm L/S. The location of the 32nm L/S in the modules is indicated by the red arrows.

The CD at 5 positions in the slit was measured using the Hitachi CG 4000 CD SEM. The results are shown in Figure 16 below. The CD is found to be constant across slit for all spacings, except for slit position $X = 12.72\text{mm}$. The actual grating that was measured is shifted 245 / 262.5 μm w.r.t. the center of the module, which means it is located 35 (H) / 17.5 (V) μm from the edge of the image field. For slit position $X = -12.72\text{mm}$ the opposite is valid, which means, the X-position of the grating is 525 (H) / 542.5 (V) μm from the edge of the image field. Both plots show a steep drop in CD from 32 to $\sim 24\text{nm}$ around $\sim 500\text{-}600\mu\text{m}$ distance from the neighboring field.

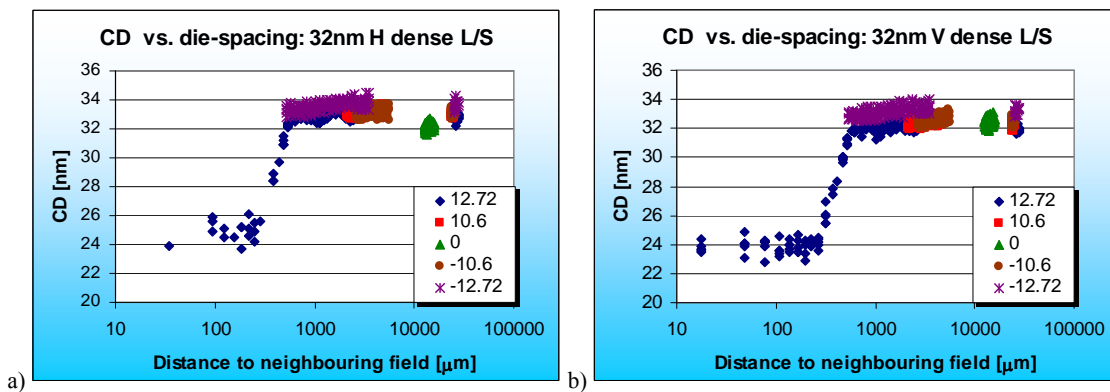


Figure 16 Measured wafer CD of 32nm L/S for 5 positions across the slit for increasing die-spacing. a) Horizontal L/S, b) vertical L/S

By selecting slit position $X = 12.72\text{mm}$ it is possible to plot the CD as function of die-spacing / distance to the neighboring field, which is done in Figure 17. The plot shows a (relatively) flat CD curve around 24nm

from 0 to $\sim 250\mu\text{m}$. The region between $250\mu\text{m}$ and $\sim 550\mu\text{m}$ shows an increase in CD to 32nm , after which the CD remains constant within the measurement noise. The transition region corresponds to the REMA half shadow. The REMA blades are positioned around $250\mu\text{m}$ from the edge of the image field. The CD difference between the area $0\text{-}250\mu\text{m}$ and $550\text{-}3000\mu\text{m}$ is 8.1nm for both H and V. This CD difference can be attributed to the EUV flare level from the absorber in the black border area, the EUV flare level from the lens and out-of-band DUV flare from the absorber. The resist that was used has a measured flare sensitivity of $1.3\text{nm}/\%$ flare¹⁰. Thus a flare level of 6.2% can be derived from the measured CD drop of 8.1nm . From the reticle design we estimated an EUV flare level of $\sim 4\%$ inside the grating, decreasing to $0.2\text{-}0.4\%$ $40\mu\text{m}$ outside the grating, based on the point spread function from the ADT lens. The out-of-band DUV flare is estimated to be $\sim 0.8\%$, based on dedicated experiments performed on this exposure tool using the same resist¹¹. Therefore the estimated EUV flare level from the absorber is $\sim 5\%$, which is slightly higher than the simulated $3.6\text{-}4.7\%$. This could be due to the optical density (k-value) assumed in the model, which appears to be higher than what can be derived from other publications⁸.

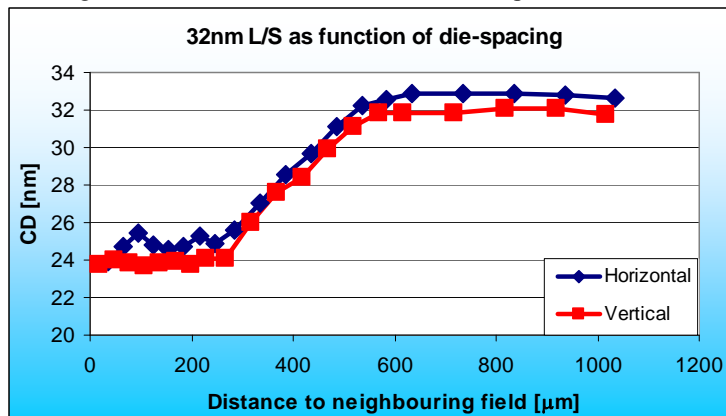


Figure 17 Measured wafer CD of 32nm L/S for increasing die-spacing.

To prevent a CDU impact from field-to-field the reticle black border should have an extremely low EUV reflectivity ($< 0.1\%$), which can only be achieved by a very thick absorber, a special coating or etching away the entire ML in the black border area, as suggested by Kamo et al⁹. However, the CD impact can also be minimized by means of OPC, using an EUV and out-of-band DUV flare model based on the PSF and REMA blade configuration from the exposure tool. The result of this model as implemented in Brion's Tachyon NXE model is shown in Figure 18 below. The simulated impact of EUV and out-of-band DUV reflections in the mask black border area is found to be well correctable using an 'exposure tool' aware model, which was the TWINSCAN NXE:3100. Work is ongoing to demonstrate this in resist.

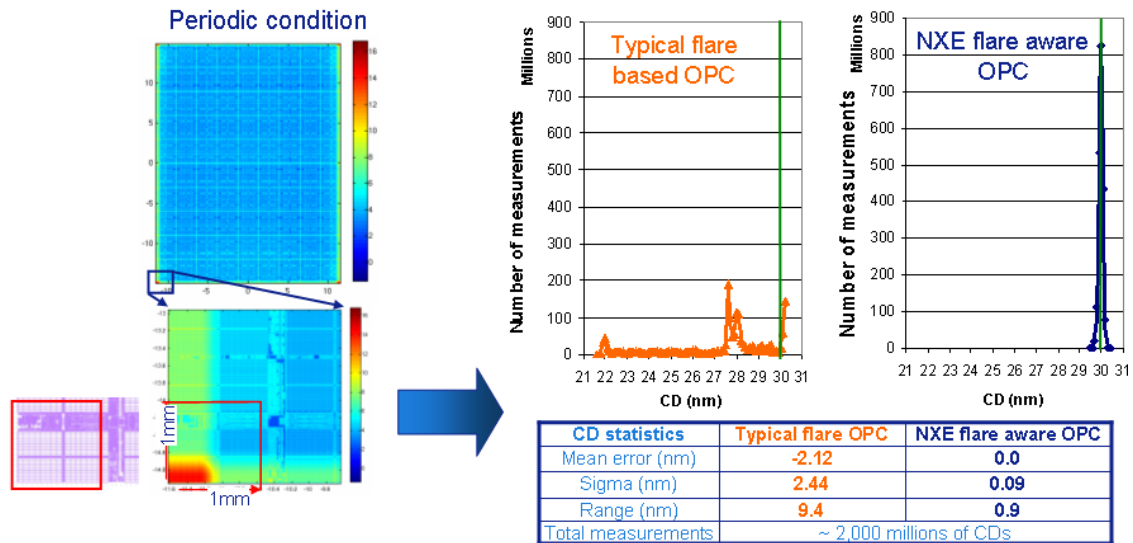


Figure 18 Simulated CDU including field boundary CD errors due to mask black border reflections with and without flare model that takes reticle reflections into account. The ‘NXE:3100 flare aware’ model is found to reduce the impact of mask black border reflections adequately.

5. Summary and conclusions

The CD swing curve as function of mask absorber height was verified experimentally for 27nm dense L/S using the MeRiT HR 32 reticle repair tool. The CD impact of absorber height variations can be minimized by choosing the correct nominal absorber thickness. Optimizing the mask stack as a whole can improve the imaging performance or relax mask making requirements. It was demonstrated that the absorber height impacts dense-iso bias and needs to be taken into account for OPC determination. For a state-of-the-art mask an absorber thickness variation of 0.5nm range across the mask was measured. The estimated CDU impact due to absorber thickness variations for such a mask is < 0.5nm, the dense-iso bias is <0.3nm.

No CD impact was observed of EUV absorber flare outside reticle black border area. To prevent a CDU hit inside the reticle black border area it needs to be very dark ($R < 0.1\%$), which is challenging from a mask making point of view. However, it is possible to compensate for these field boundary CD errors by means of an ‘exposure tool aware’ flare OPC model, as implemented in Brion’s Tachyon NXE model for the TWINSCAN NXE:3100.

6. Acknowledgements

The authors would like to acknowledge Eric Hendrickx, Jan Hermans and Gian Lorusso from IMEC, and the ASML ADT team at IMEC for support with wafer exposures. We thank Brid Connolly from Toppan Photomasks and Johannes Ruoff from Carl Zeiss for valuable input, Hua-yu Liu and Keith Gronlund from Brion for sharing data from the Tachyon NXE model. We would also like to thank Yin Fong Choi and Mariette Berende for the extensive CD SEM measurements, and Andre van Dijk, Yue Peng, John Zimmerman and Noreen Harned for fruitful discussions.

¹P.Y. Yan, The Impact of EUVL Mask Buffer and Absorber Material Properties on Mask Quality and Performance, Emerging Lithographic Technologies VI, Proc. SPIE, Vol. 4688 (2002)

²E. van Setten et al, Impact of mask absorber on EUV imaging performance, Proc. SPIE, Vol. 7545 (2010)

³M. Waiblinger et al, E-beam induced EUV photomask repair – a perfect match, Proc. SPIE Vol. 7545 (2010)

⁴H. Meiling et al, “Development of the ASML EUV alpha demo tool”, Emerging Lithographic Technologies IX, Proc.SPIE, Vol. 5751 (2005)

⁵http://henke.lbl.gov/optical_constants/getdb2.html

⁶C.A.Mack, Impact of Mask Roughness on Wafer Line-Edge Roughness, Proc. SPIE Vol. 7488 (2009)

⁷J. Ruoff, Impact of mask topography and multilayer stack on high-NA imaging of EUV masks, Proc. SPIE Vol. 7823 (2010)

⁸H.S.Seo et al, Absorber stack optimization in EUVL masks: lithographic performances in alpha demo tool and other issues, Proc. SPIE Vol. 7636 (2010)

⁹ T. Kamo et al, Thin absorber EUV mask with light-shield border of etched multilayer and its lithographic performance, Proc. SPIE Vol. 7748 (2010)

¹⁰ G.F. Lorusso et al, Full Chip Correction of EUV Design, Proc. SPIE Vol. 7636 (2010)

¹¹ to be published